BlinkenArea
Licht. Schönheit. Mehr.

BlinkenWall reloaded

Extending a large LED display from 1986
to support Ethernet and Grayscales

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How it began...

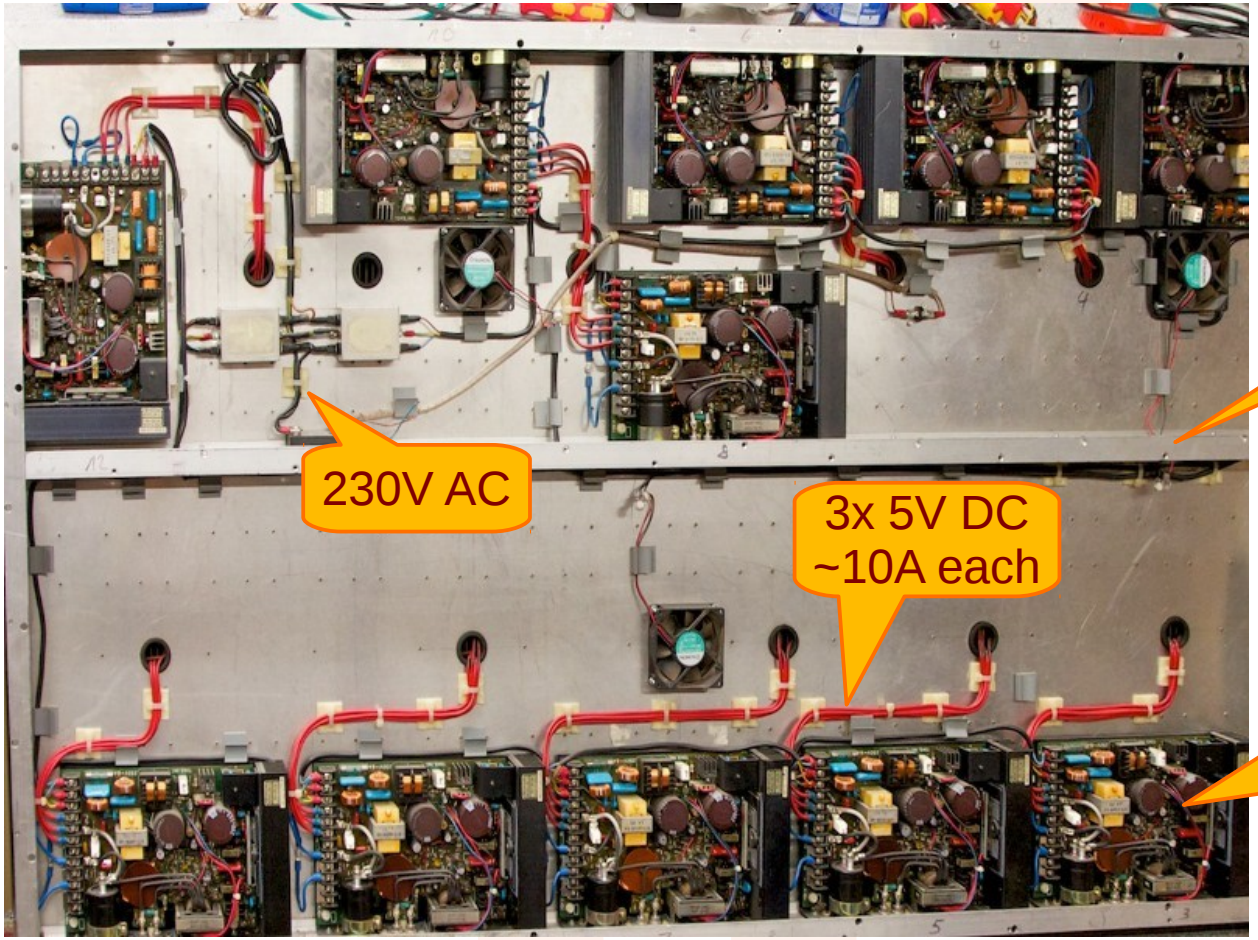
- June 10th, 2005: efelon spots LED display with ~20k LEDs in Ebay
- June 12th, 2005: ST wins the auction
- June 23th, 2005: display mounted in POC Sascha's basement

- ~2m wide, ~1 m high
- ~200 kg
- 240x96 pixels / 23040 LEDs
- not doing anything...

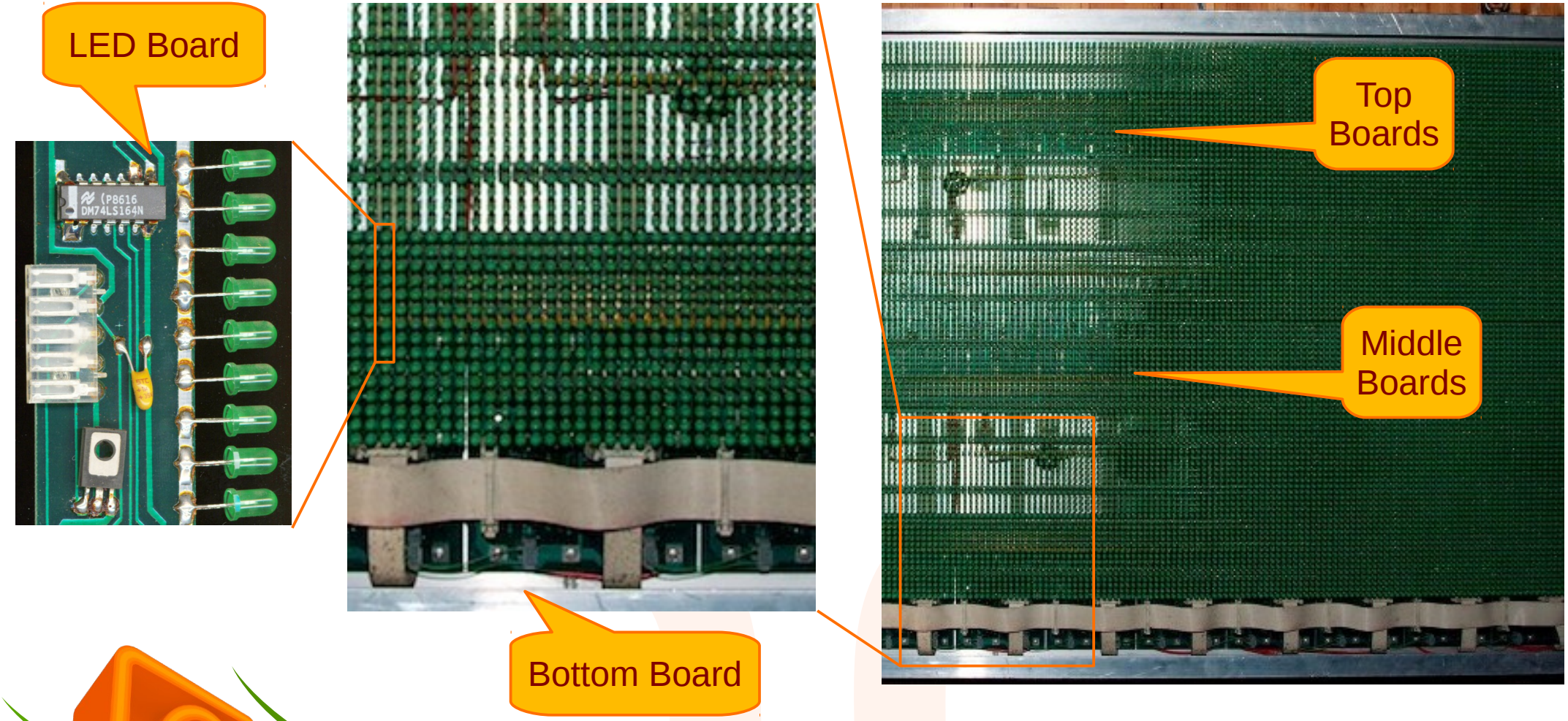
The Old Main Controller

- ~1986: old main controller is manufactured/programmed
  - multiple Z80 Processors
- 2005: old main controller is turned on again
  - update of picture: display off, … thinking …, new picture
  - not working 100% properly any more
  - dies completely after a few tries
- June 24th, 2005: reverse engineering begins

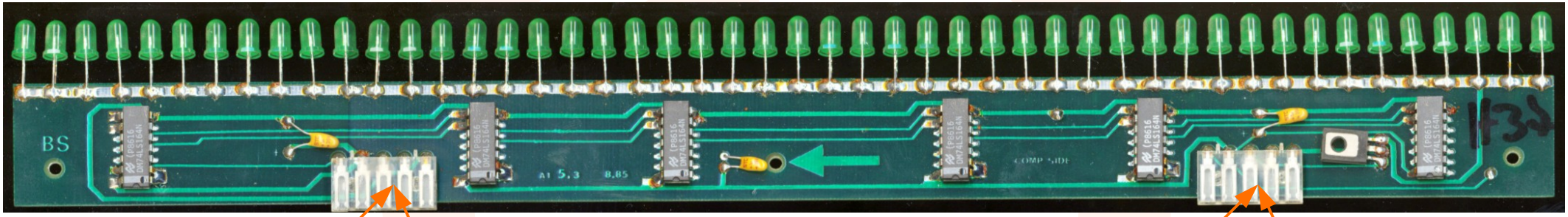
What's inside?



What's inside?



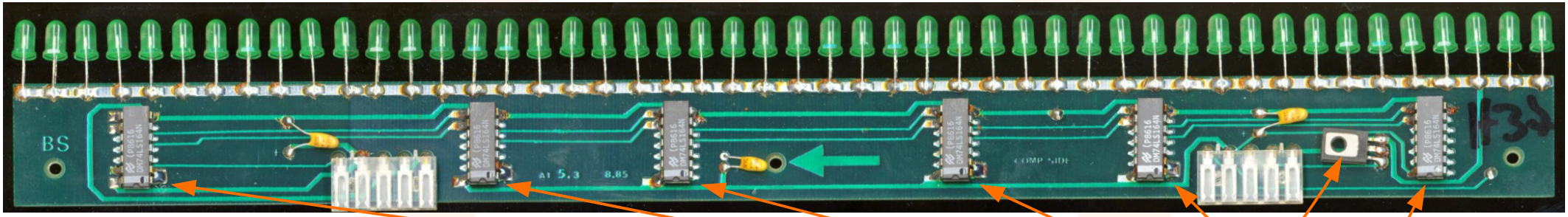
LED Board



Top Board (for upper half) Middle Board

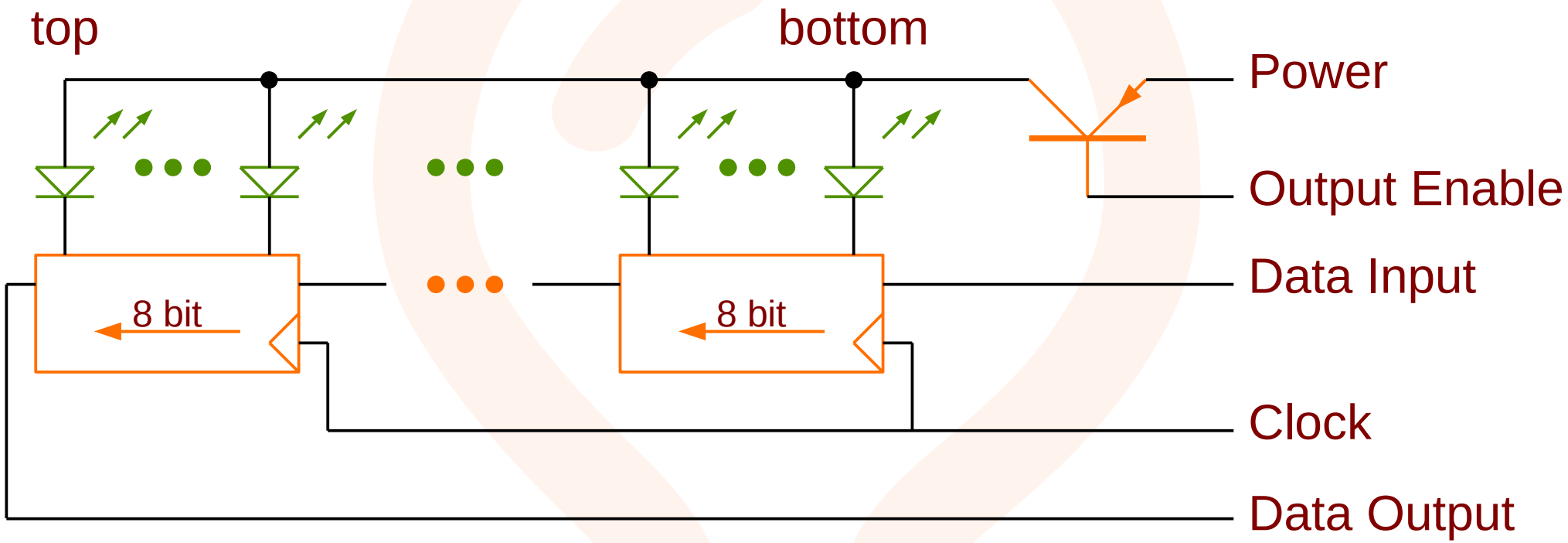
Middle Board (for lower half) Bottom Board

LED Board

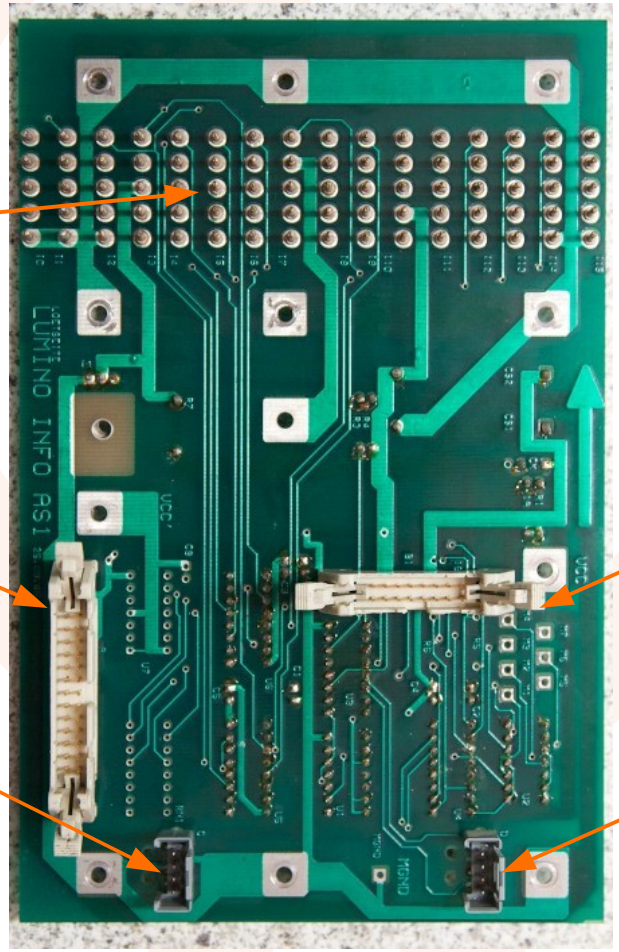


- 48x LED
- 6x 74LS164
  - 8 bit serial-in parallel-out shift register
- 1x Transistor
  - for turning off all LEDs

LED Board


top
bottom
Power
Output Enable
Data Input
8 bit
8 bit
Clock
Data Output

Bottom Board



LED Boards

Main Controller

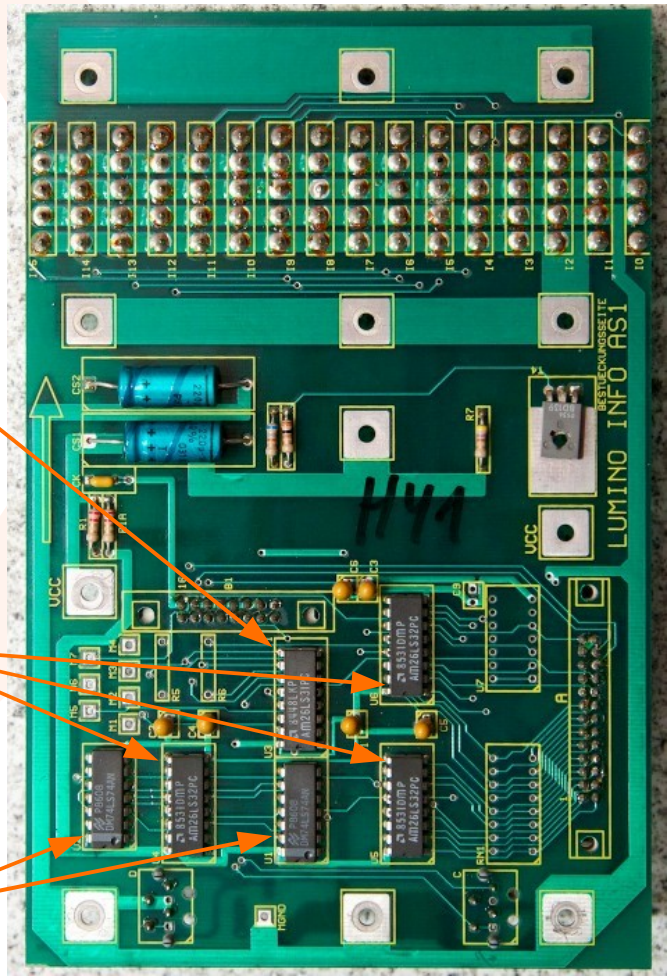
Bottom Board
(left)

Top Board
Middle Board

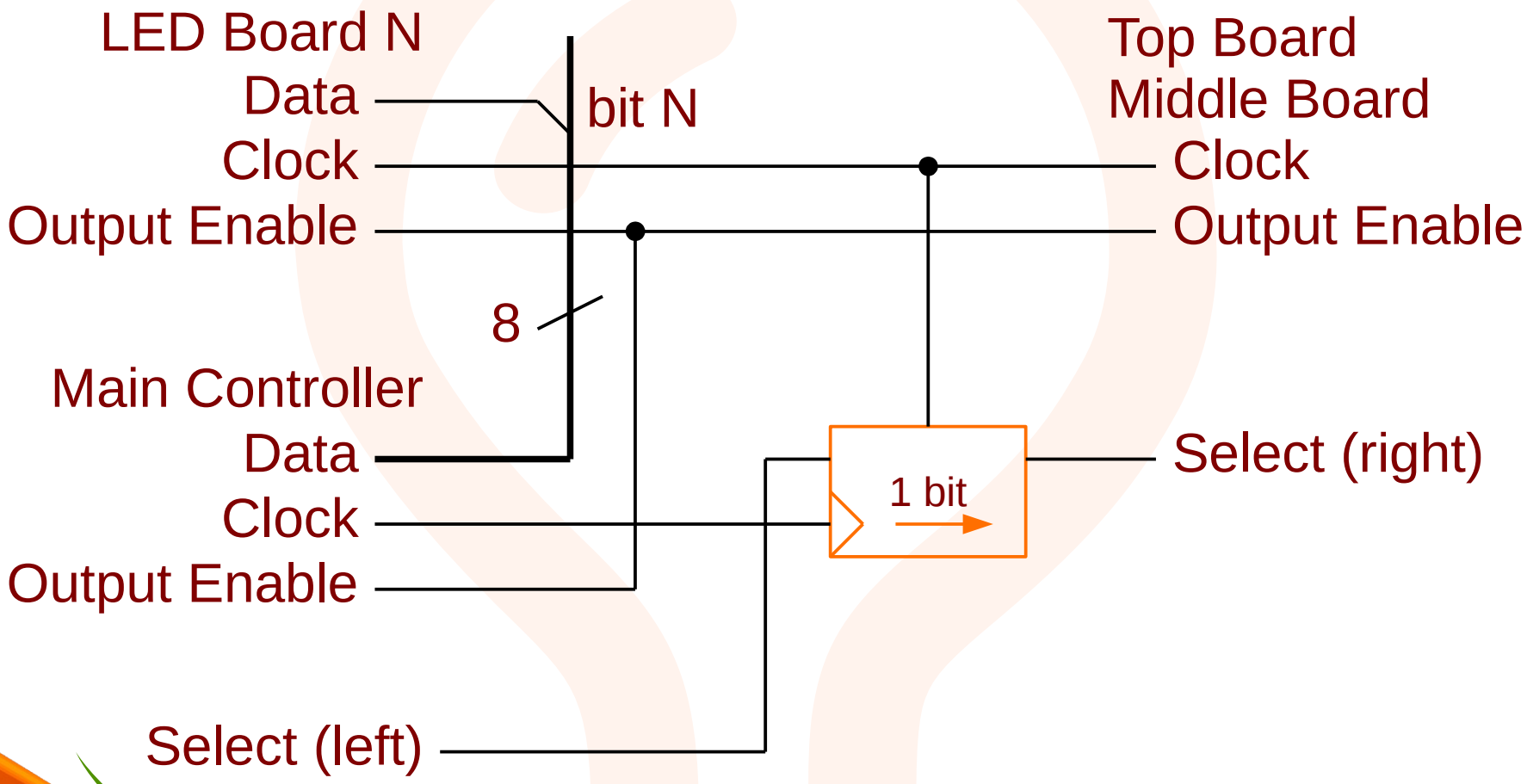
Bottom Board
(right)

Bottom Board

- 1x AM26LS31
  - differential line driver
- 3x AM26LS32
  - differential receiver
- 2x 74LS74
  - D-flipflops
  - used as 1 bit shift register

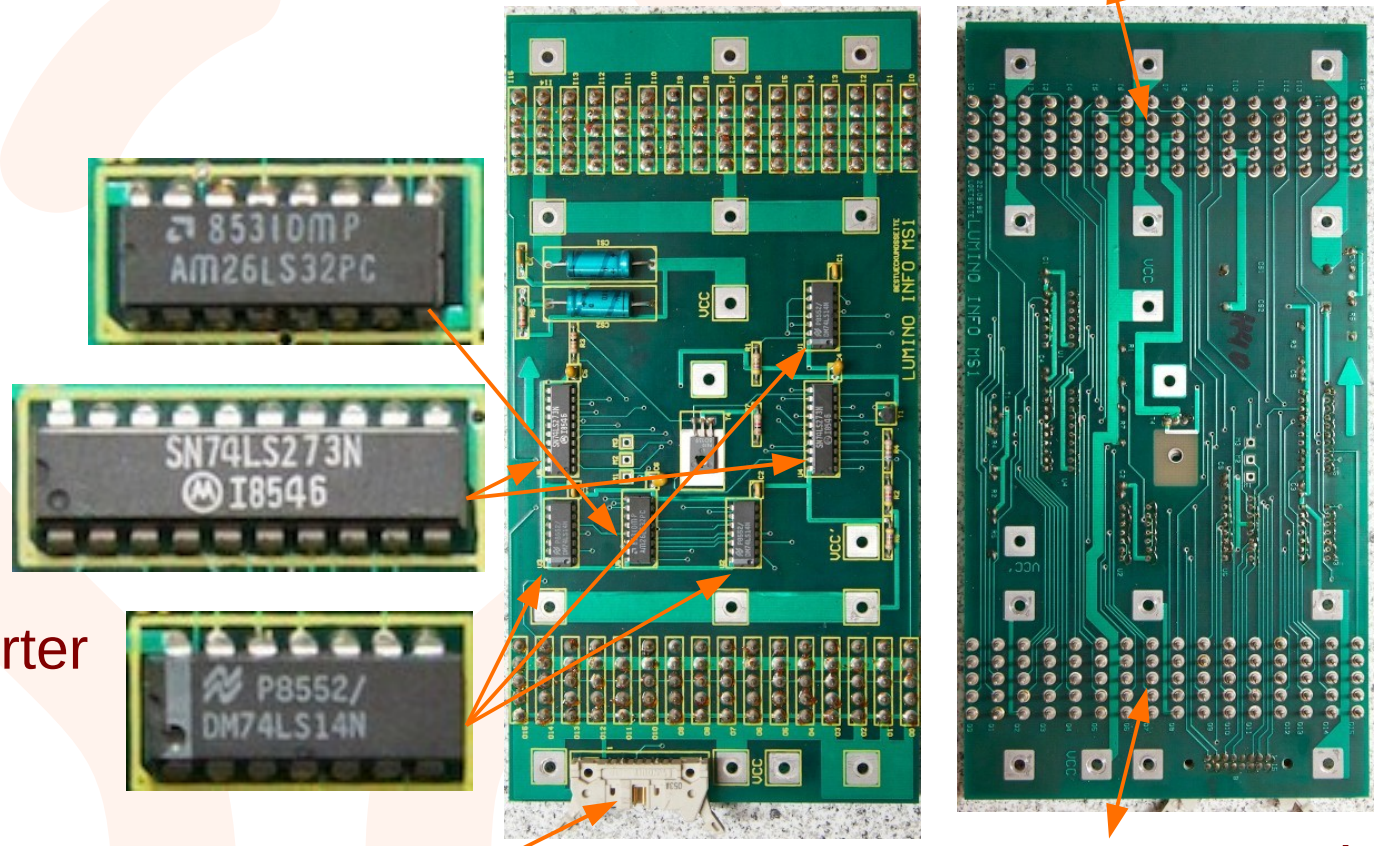


½ Bottom Board

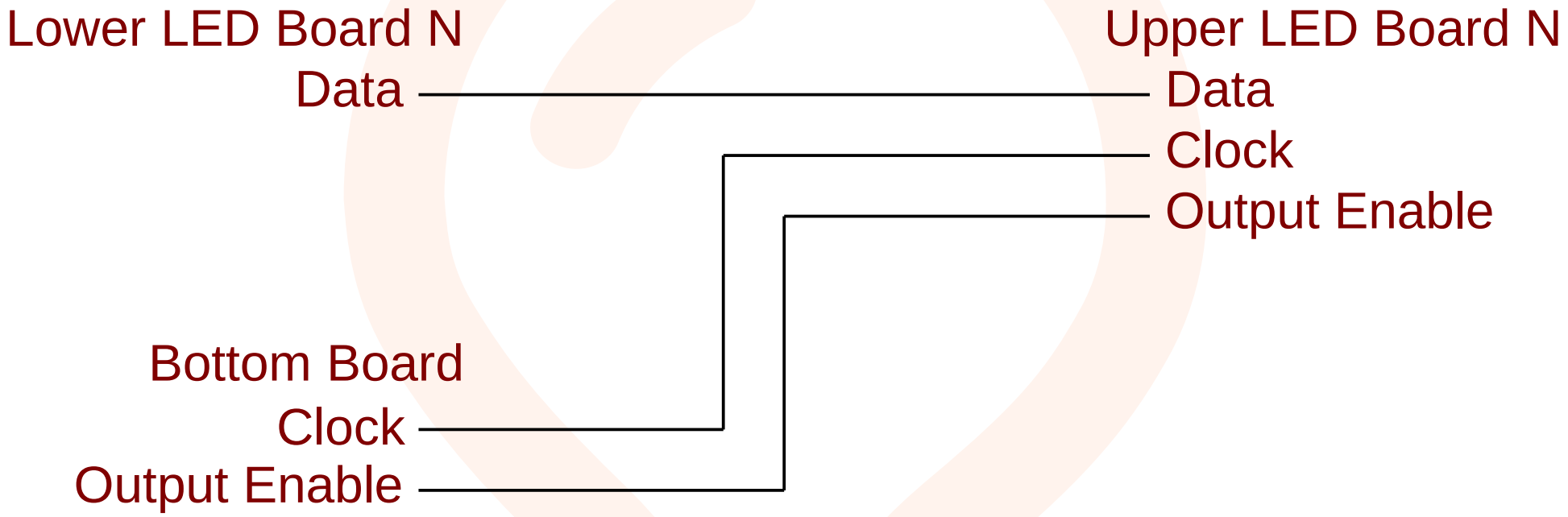


Middle Board

- 1x AM26LS32
  - differential receiver
- 2x 74LS273
  - D-flipflops
  - used as data buffer
- 3x 74LS14
  - Schmitt-Trigger Inverter
  - used as clock buffer

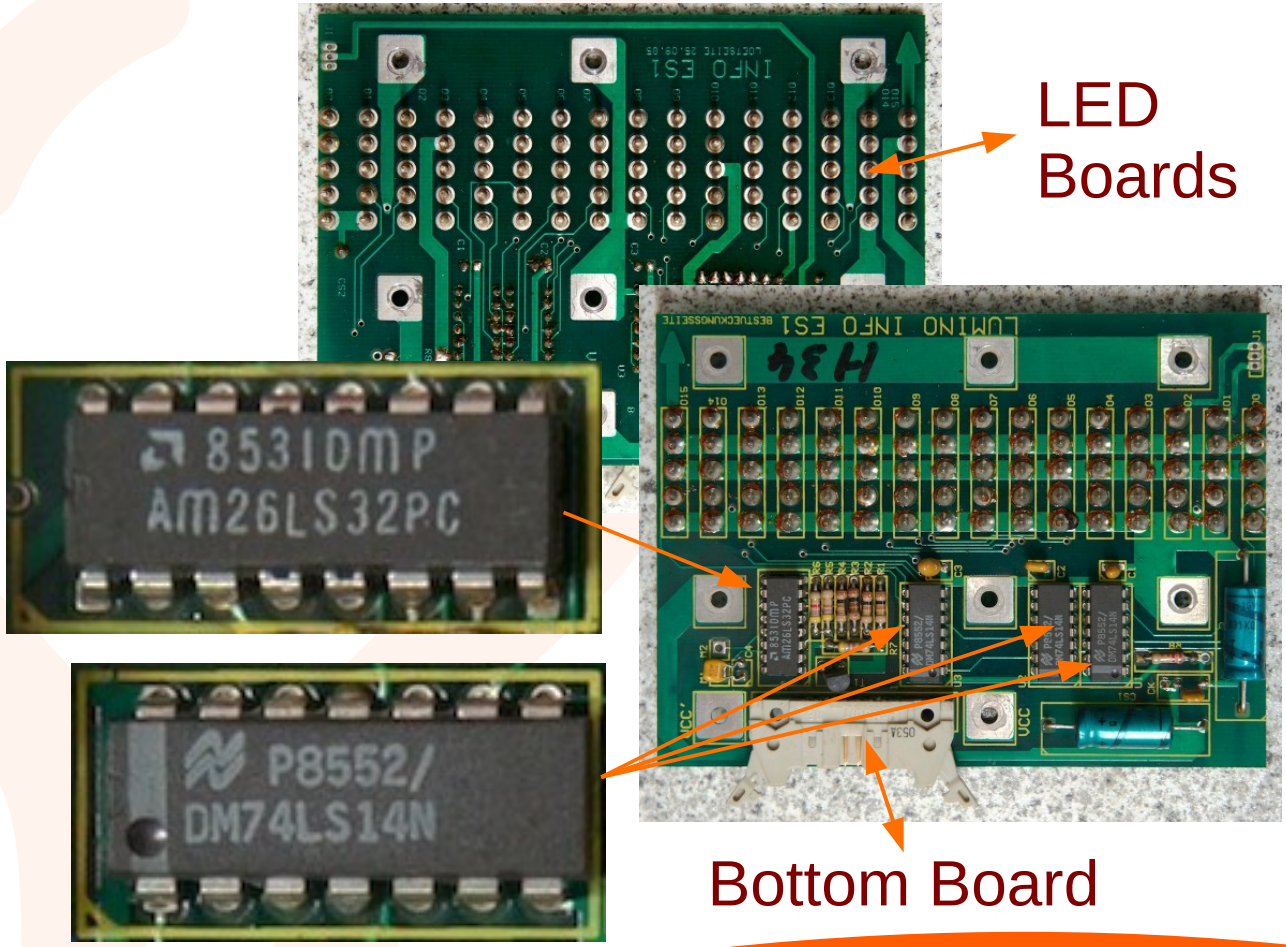


Middle Board

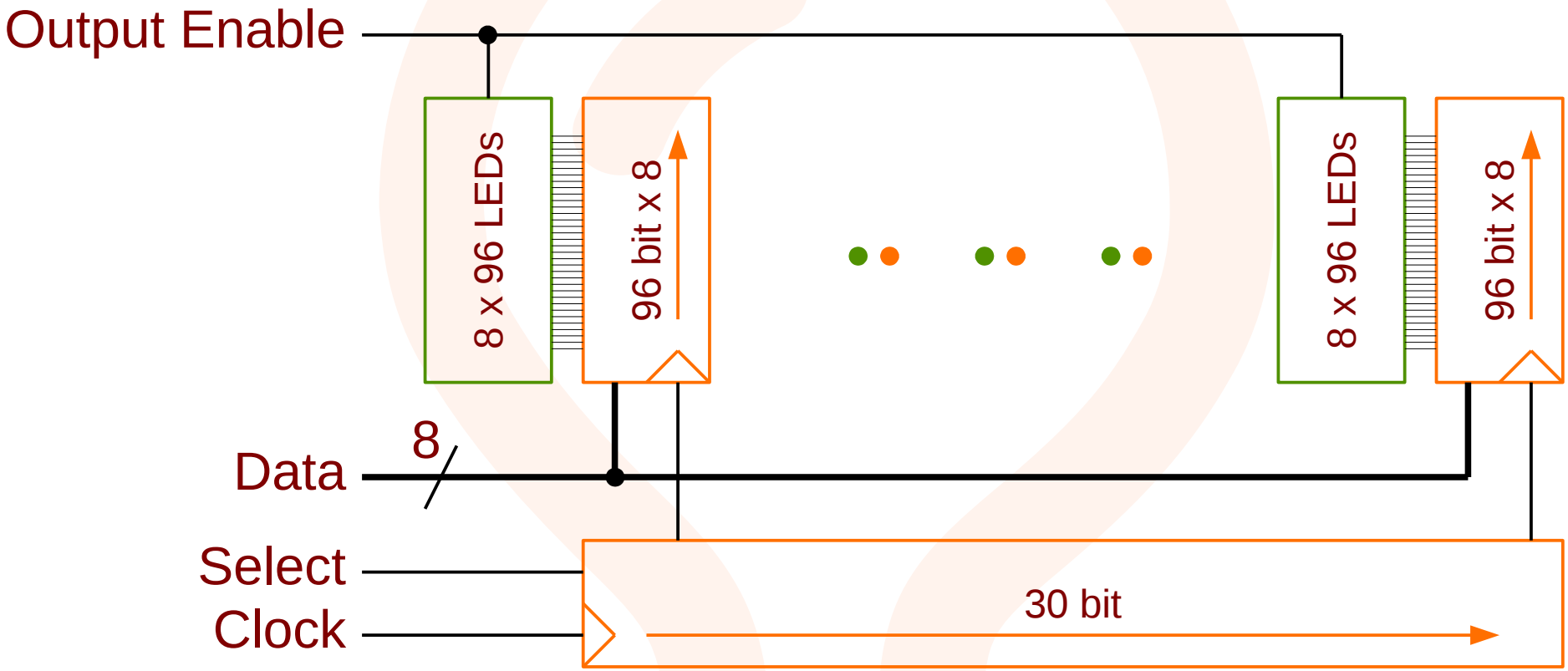


Top Board

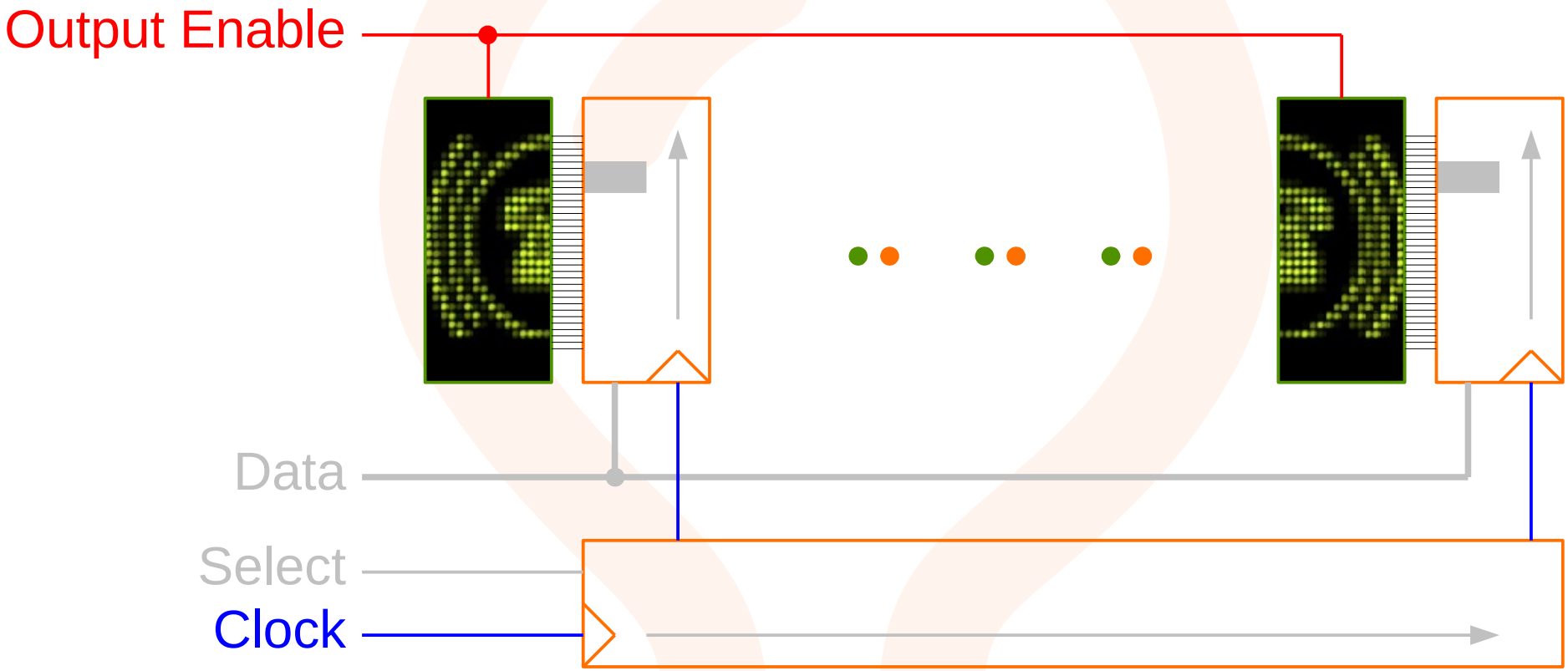
- 1x AM26LS32
  - differential receiver
- 3x 74LS14
  - Schmitt-Trigger Inverter
- Everything this board does has been simplified away for this talk. :-)



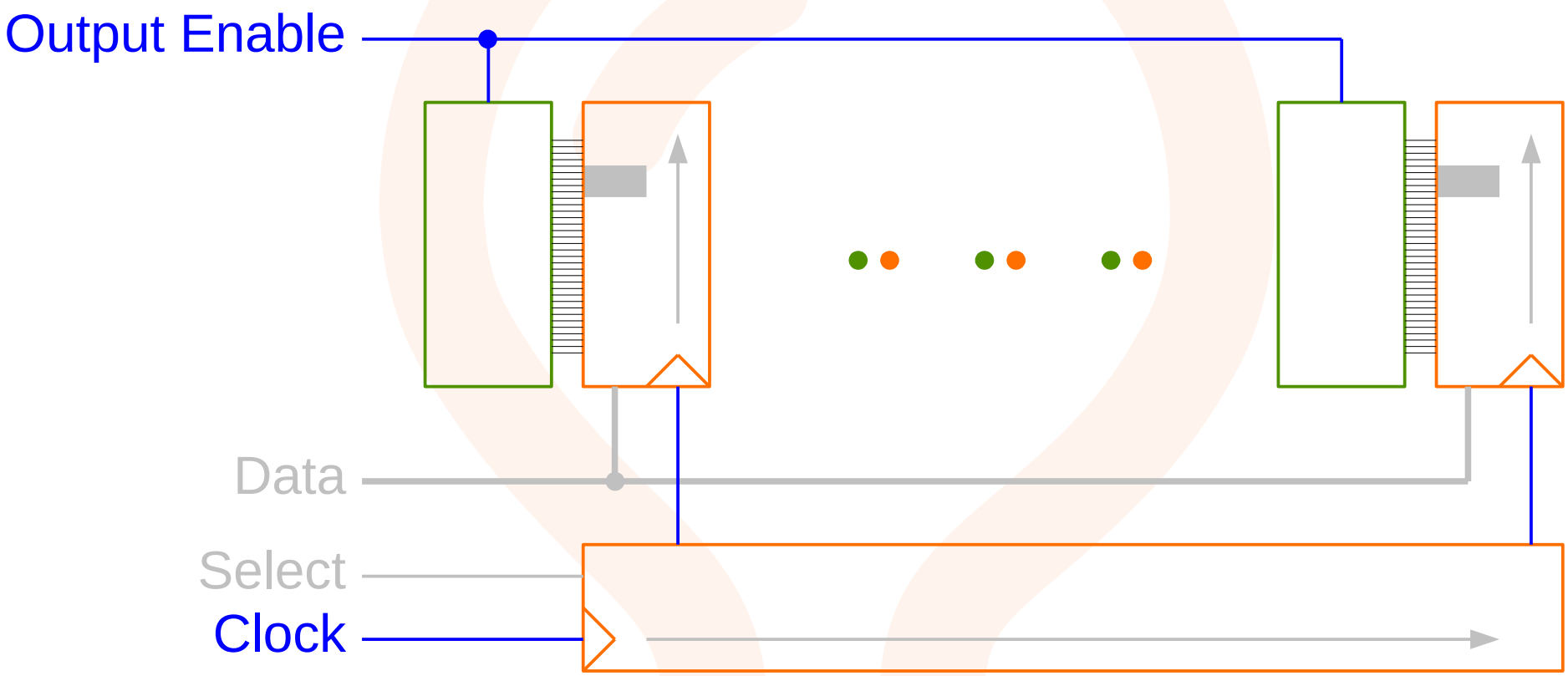
Block Diagram



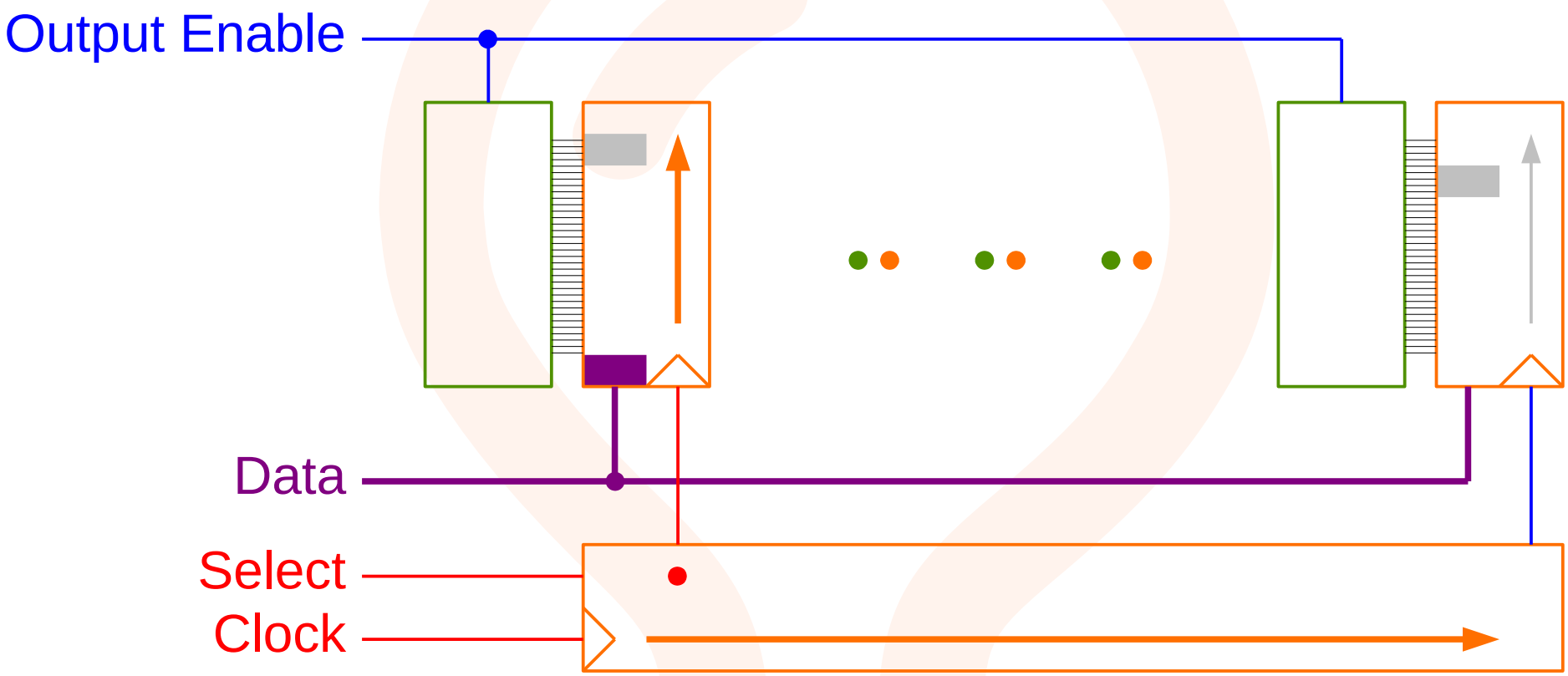
How to show a picture - idle



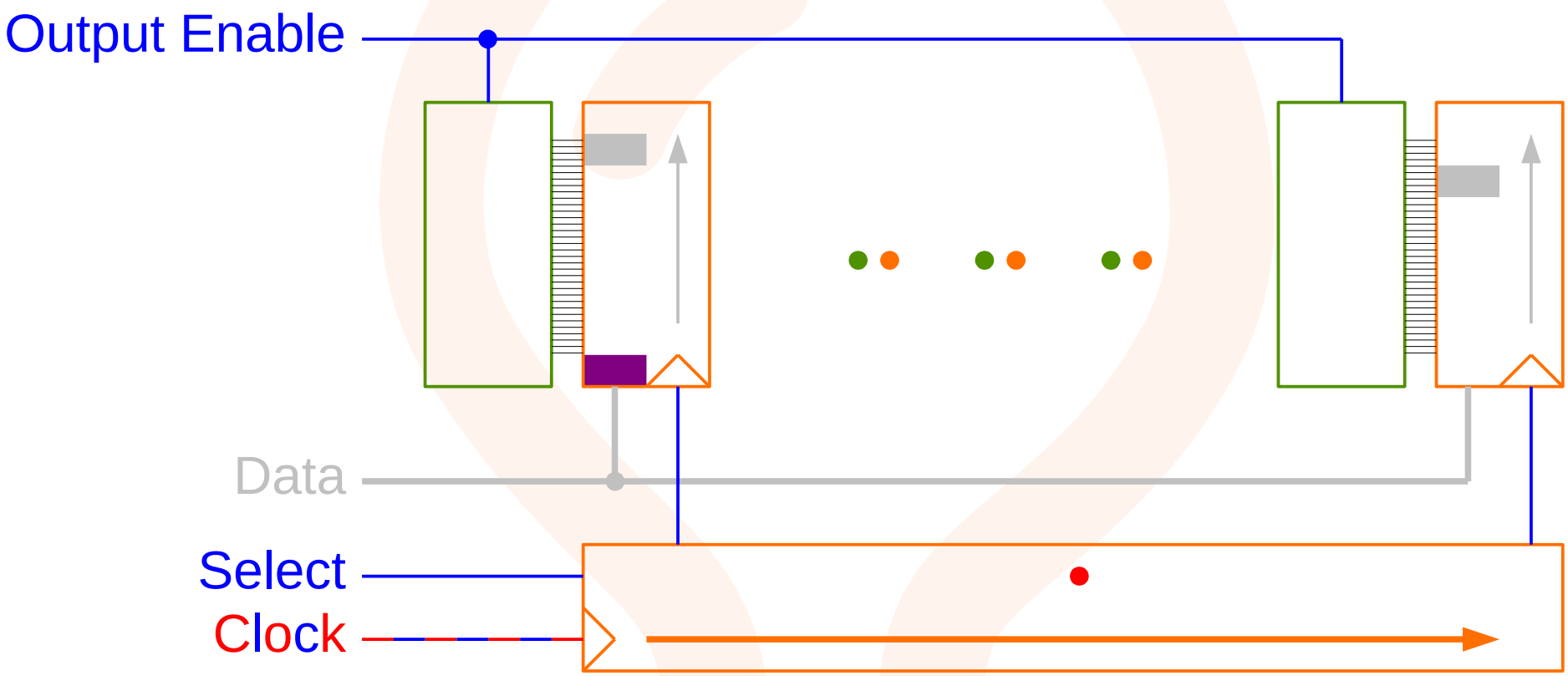
How to show a picture – turn off



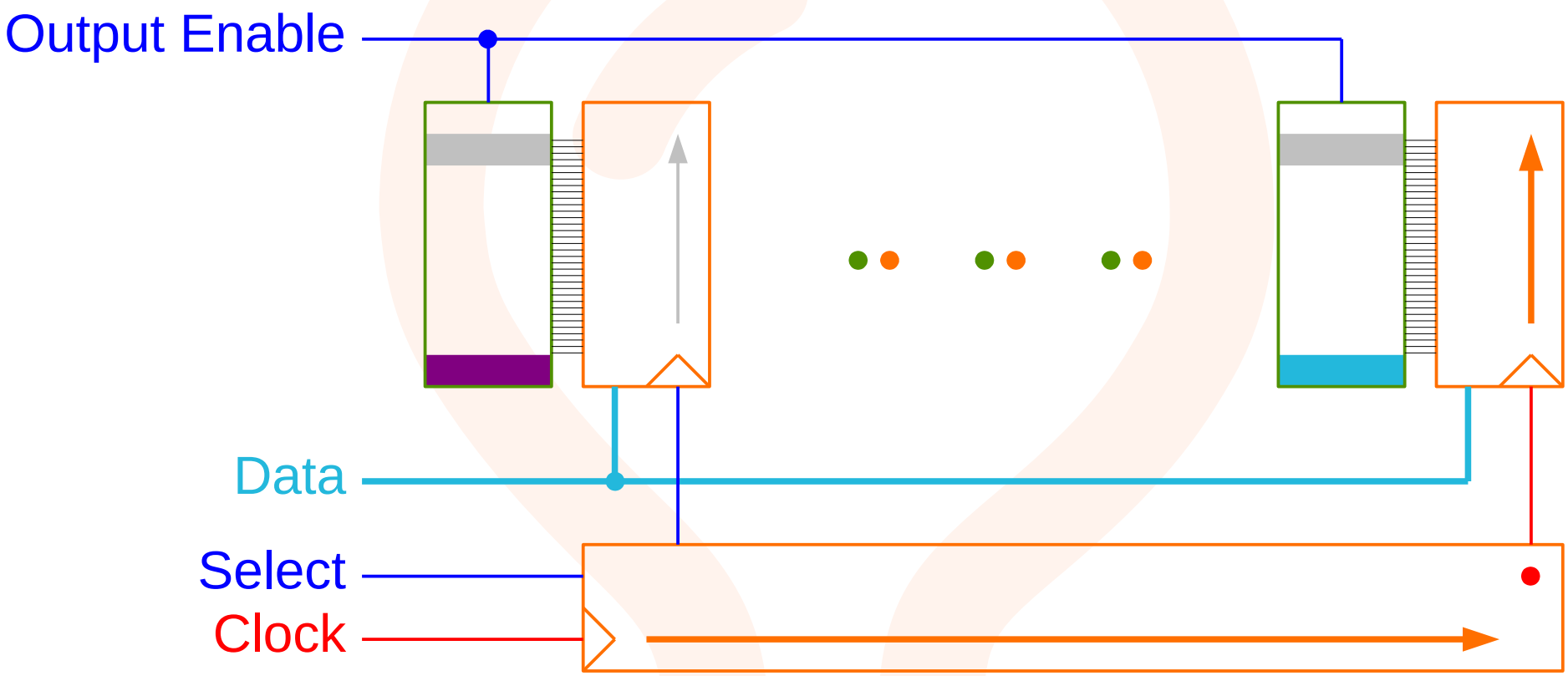
How to show a picture – top left



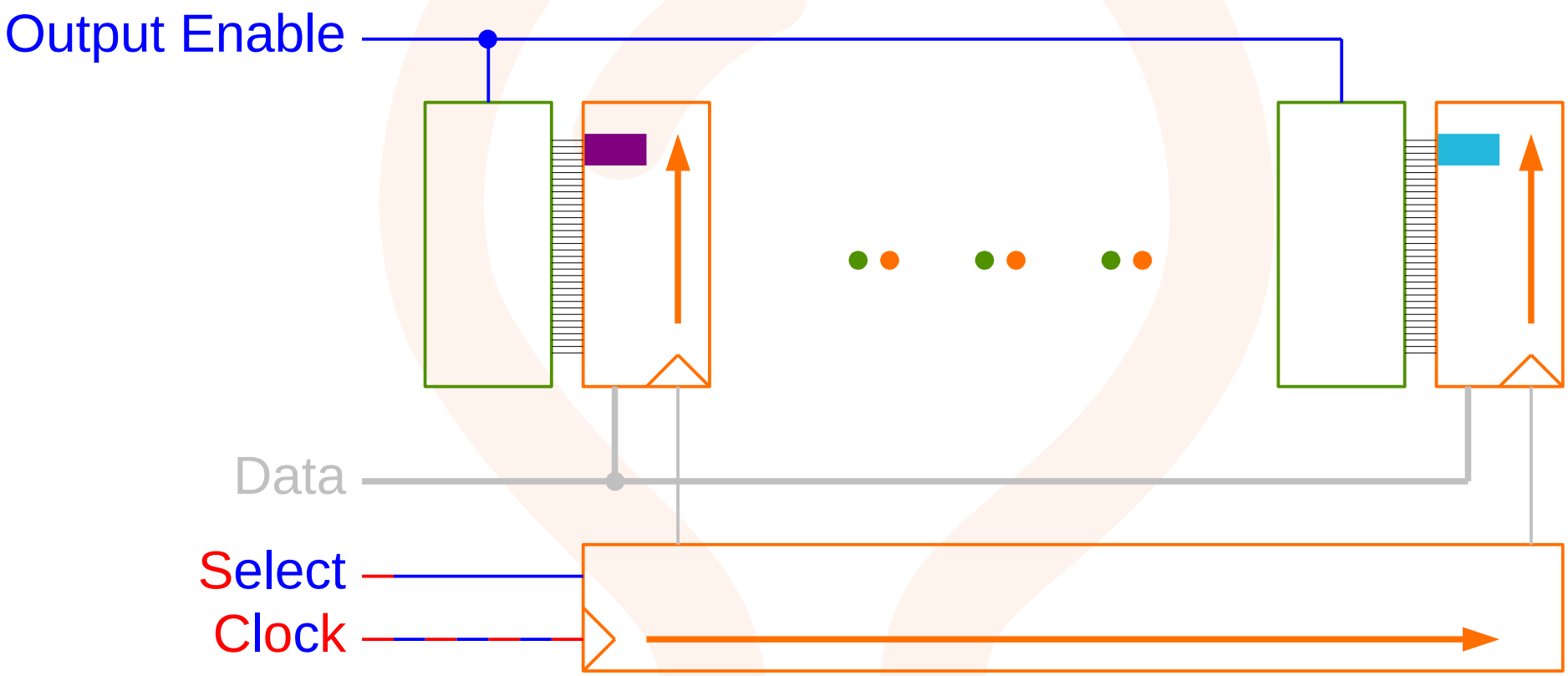
How to show a picture – top



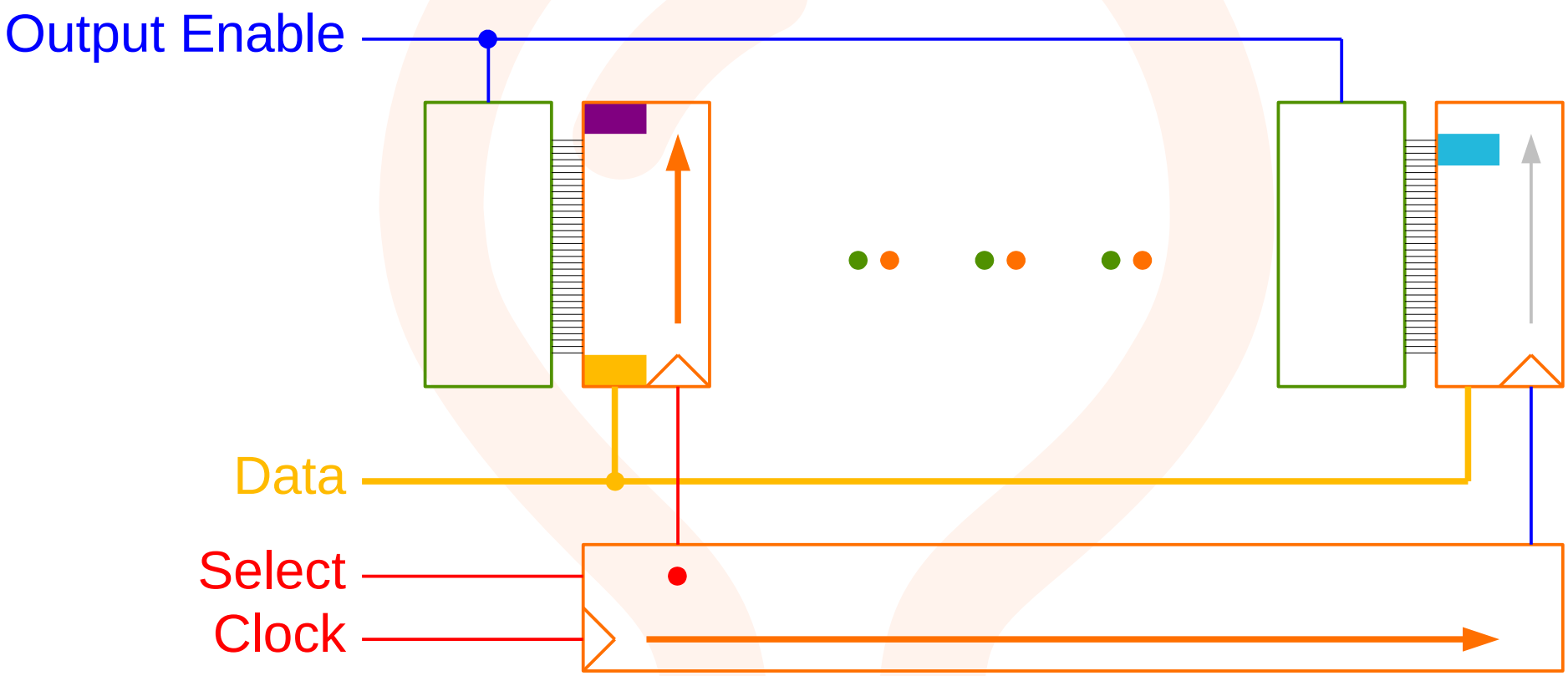
How to show a picture – top right



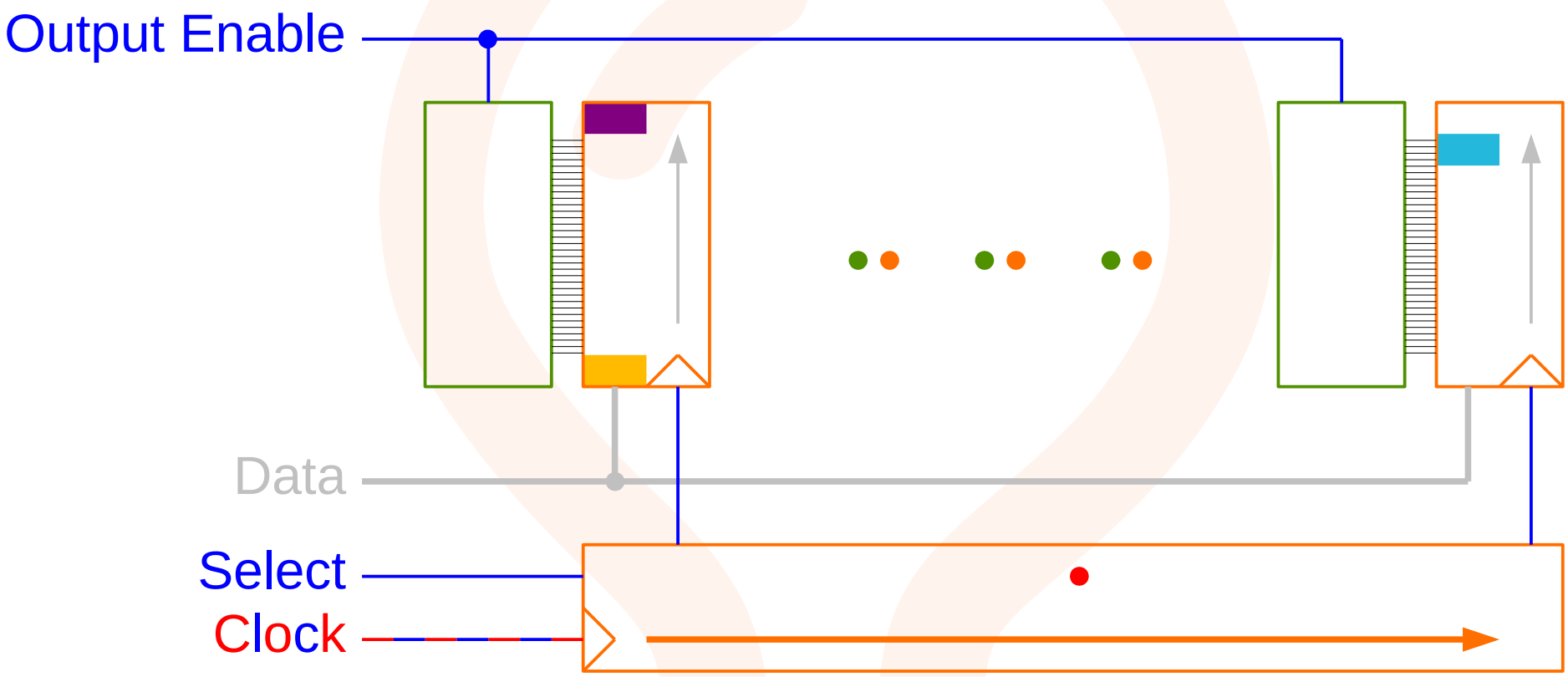
How to show a picture – more rows



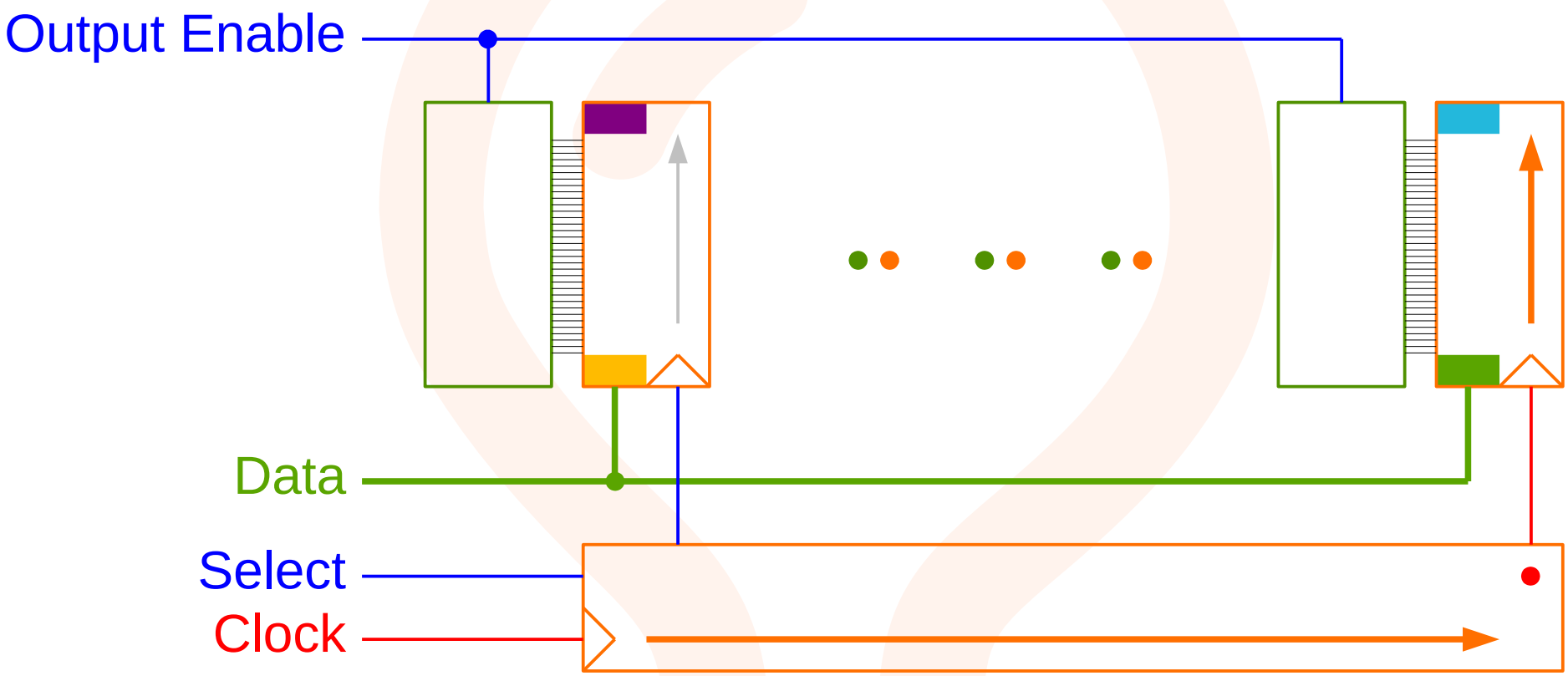
How to show a picture – bottom left



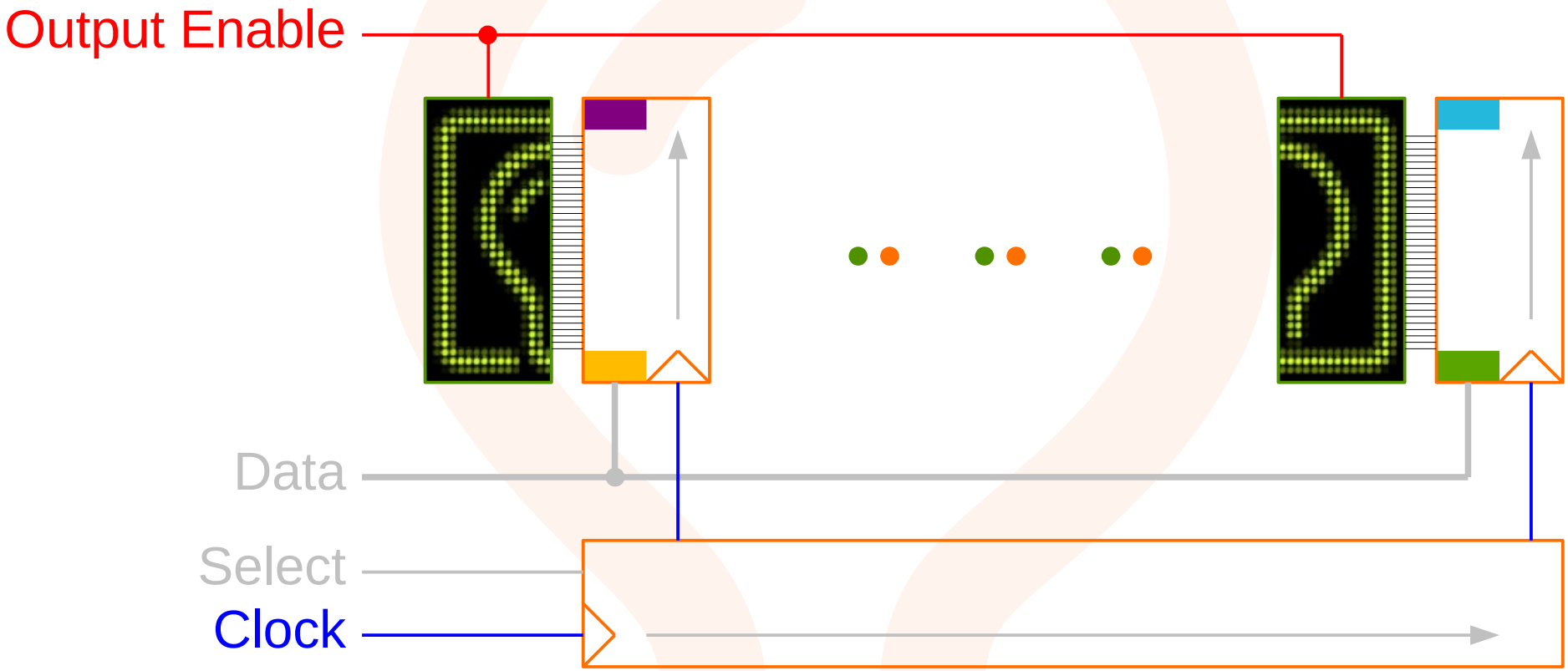
How to show a picture – bottom



How to show a picture – bottom right

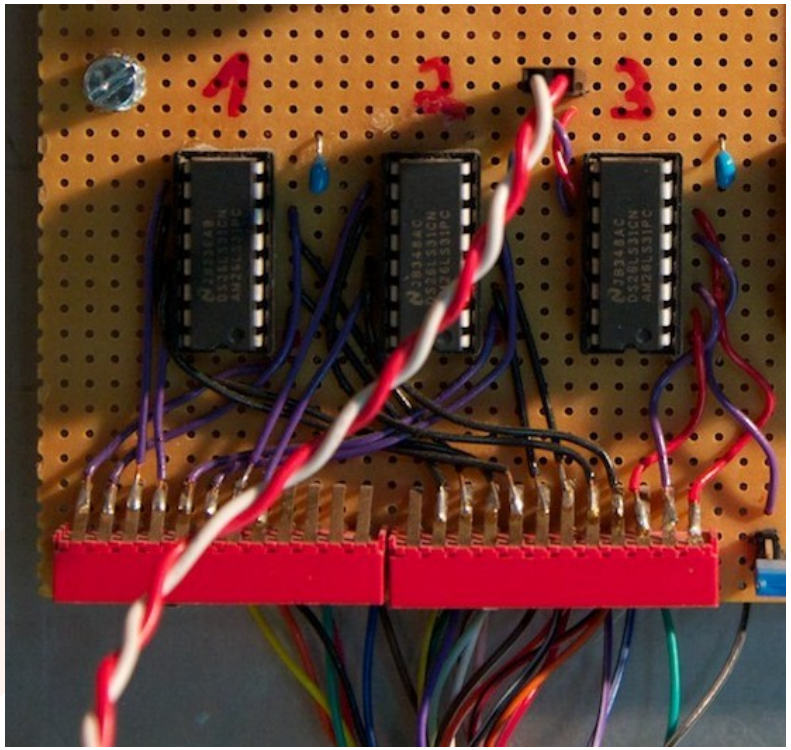


How to show a picture – turn on



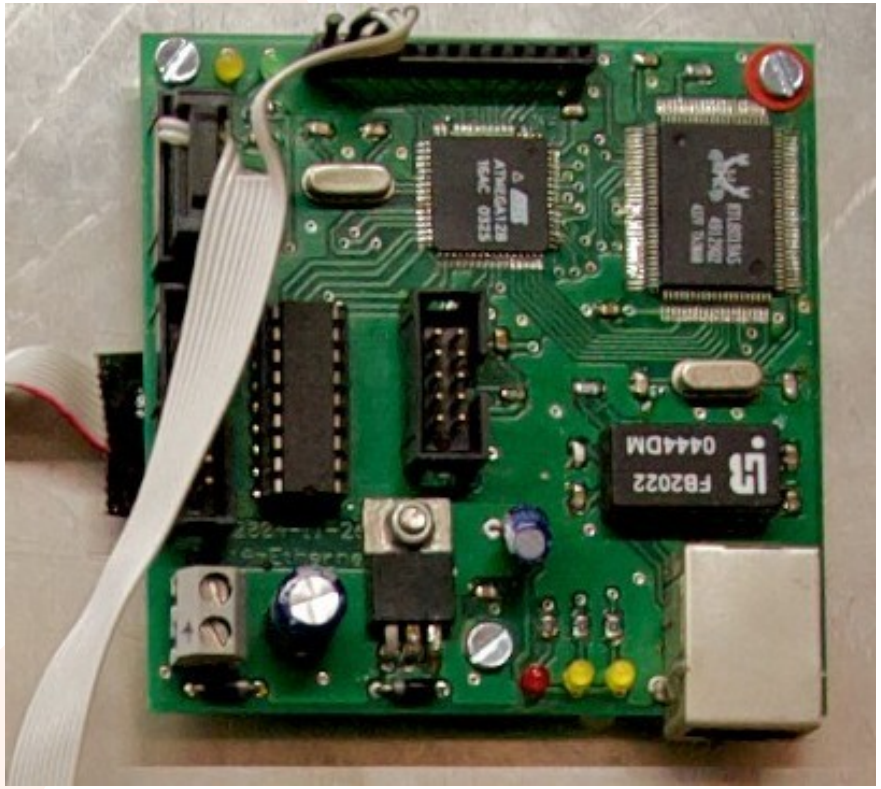
Differential Line Drivers

- How to drive the differential inputs?
  - Differential Line Drivers AM26LS31
  - Where to get those old chips?
- June 24th, 2005:
  - Sascha and Stefan enter an electronics shop
  - … and ask for AM26LS31 …
  - … and get 3x DS26LS31. :-)



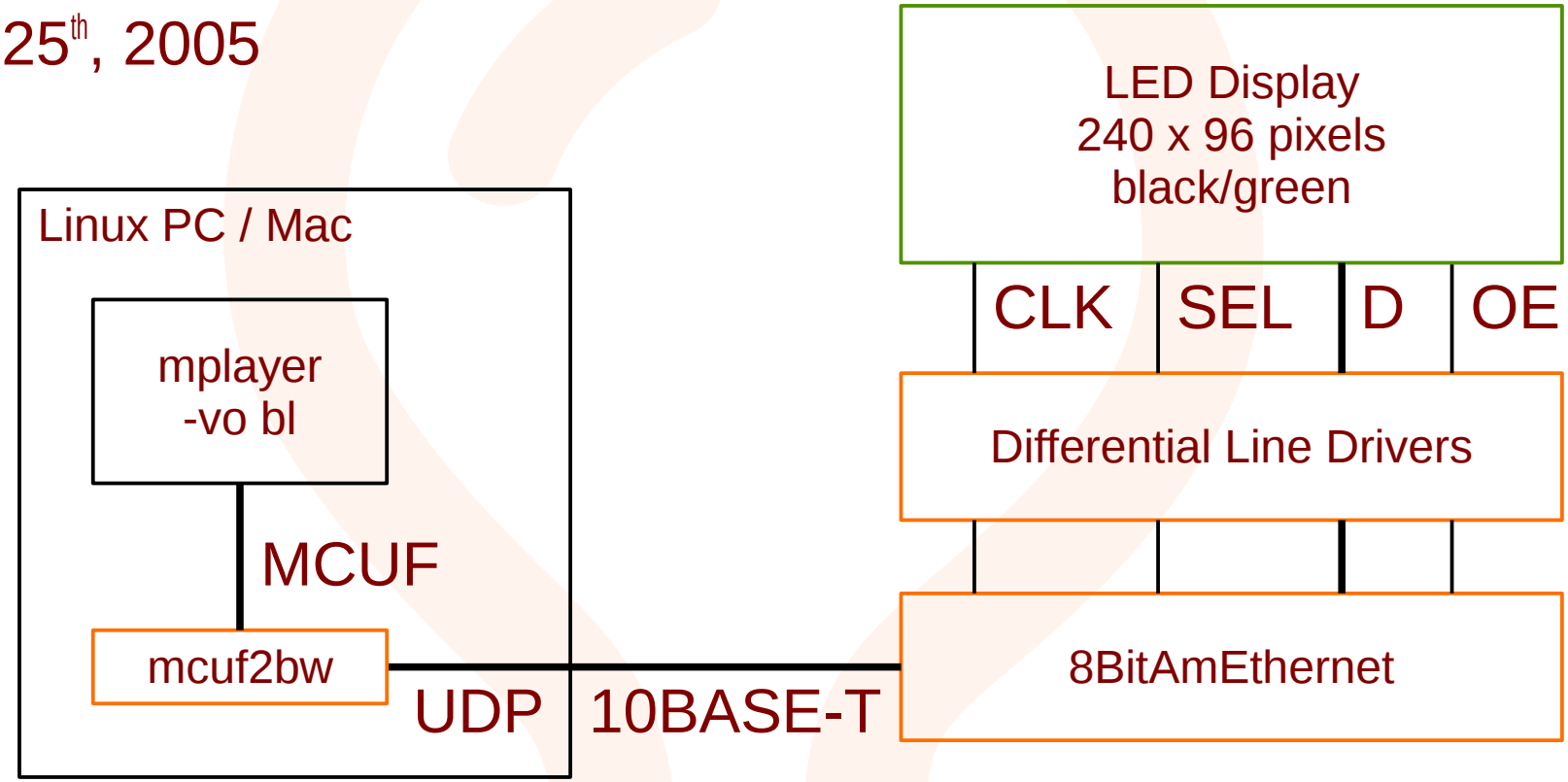
New Main Controller

- 8BitAmEthernet
  - Attaching an 8 bit AVR to Ethernet
    - 2004-2005 by Stefan + CCCAC
  - ATMEGA128 Microcontroller
    - 16 MIPS
    - 128 kB Flash
    - 4 kB SRAM
  - RTL8019AS Ethernet Controller
    - 10BASE-T
  - Some I/O Pins

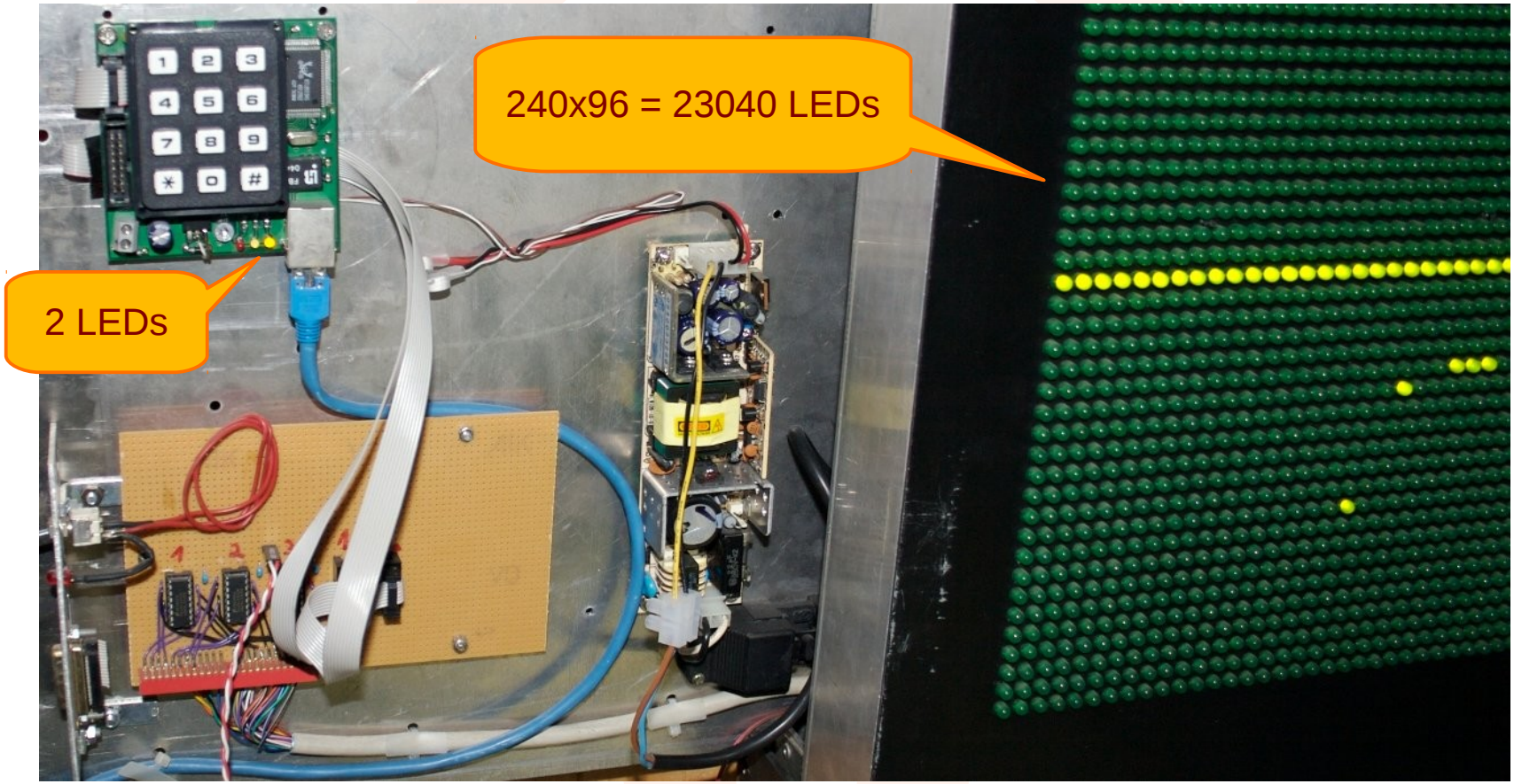


BlinkenWall is born

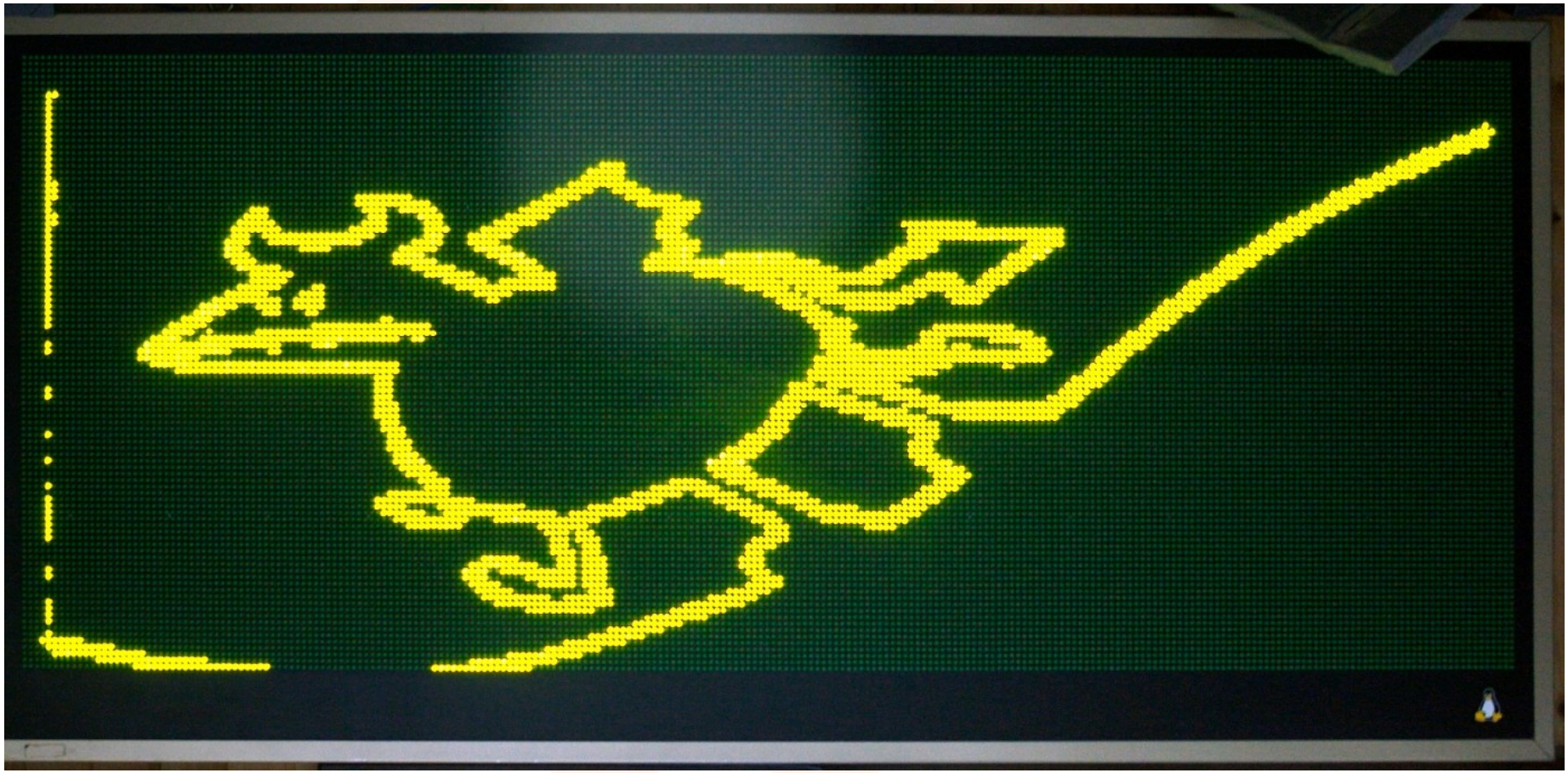
- June 25th, 2005



BlinkenWall Controller



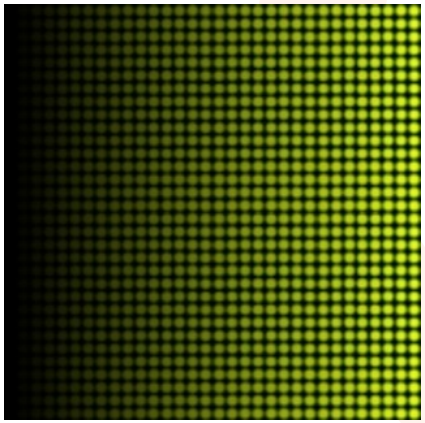
Black/Green Video



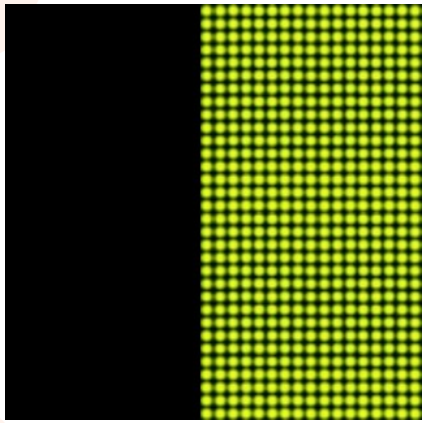
BlinkenWall @WTH2005

Dithering

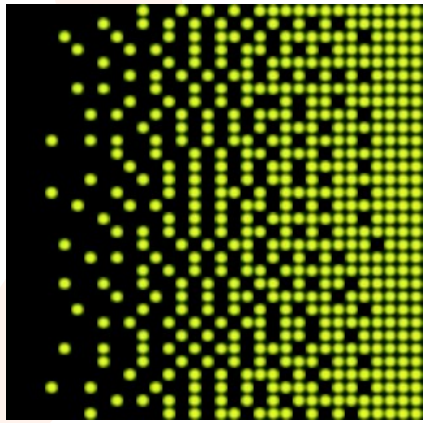
- HAR2009: Floyd-Steinberg Dithering (on PC)



Greenscale Picture (not supported)



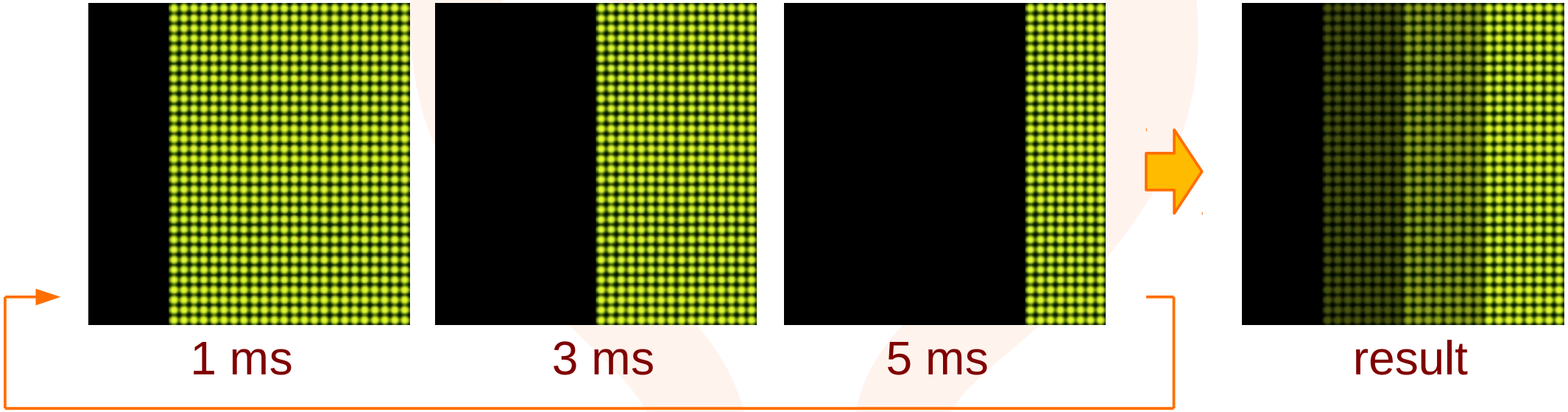
black/green



Floyd-Steinberg Dithering

How to do Grayscales?

- Pulse Width Modulation
  - Output b/w pictures faster than the human eye can follow: > 80Hz



Are Grayscales Possible?

- Outputting 8 pixels: 3 steps
  - 1) set data + set/clear select 2) set clock 3) clear clock
- Outputting a row – 30x 8 pixels: 90 steps
- Outputting a picture – 96 rows: ~ 9k steps
- Chips in Display
  - propagation delay: < 36 ns
  - time for 9k steps: 324 µs

Grayscales should be possible...

How many Greyscales?

- Time to output a b/w subframe: o = ~ 0.3 ms
  - display is dark
- Number of grayscales: N
- Time of first subframe: t
- Frequency: f = 80 Hz

$$f = \frac{1}{(N-1)\cdot o + \sum_{i=1}^{N-1} (2\cdot i - 1)\cdot t}$$

$$t = \frac{\frac{1}{f\cdot(N-1)} - o}{N-1}$$

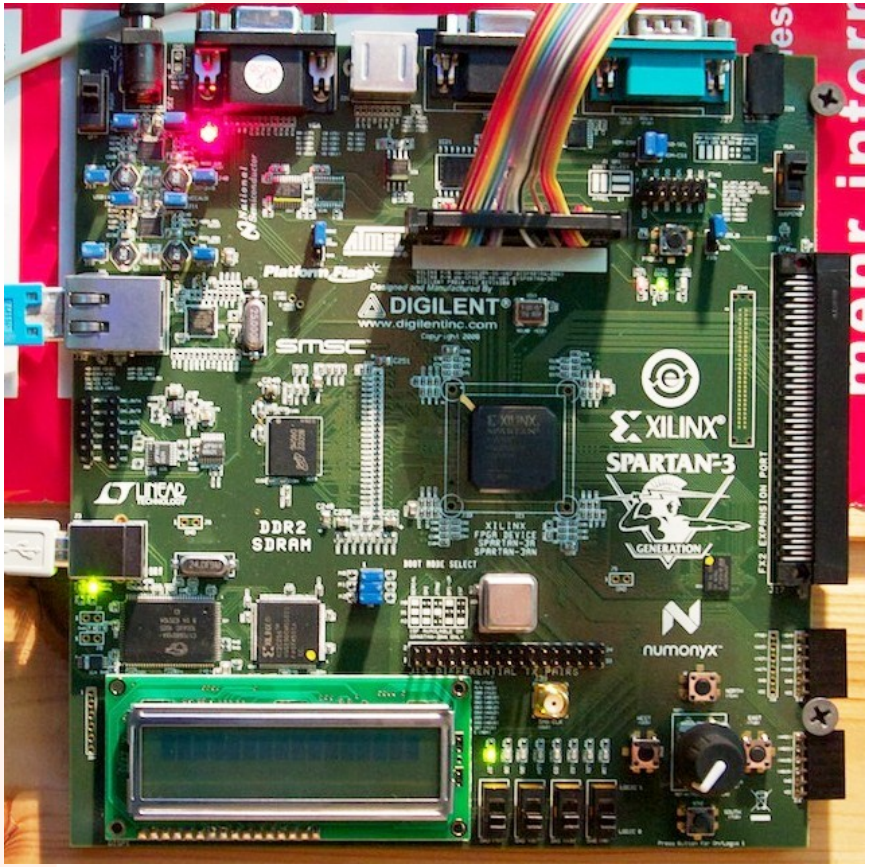
N	t
2	~ 12 ms
4	~ 1.3 ms
8	~ 0.2 ms
16	~ 36 µs

Finding a Processor

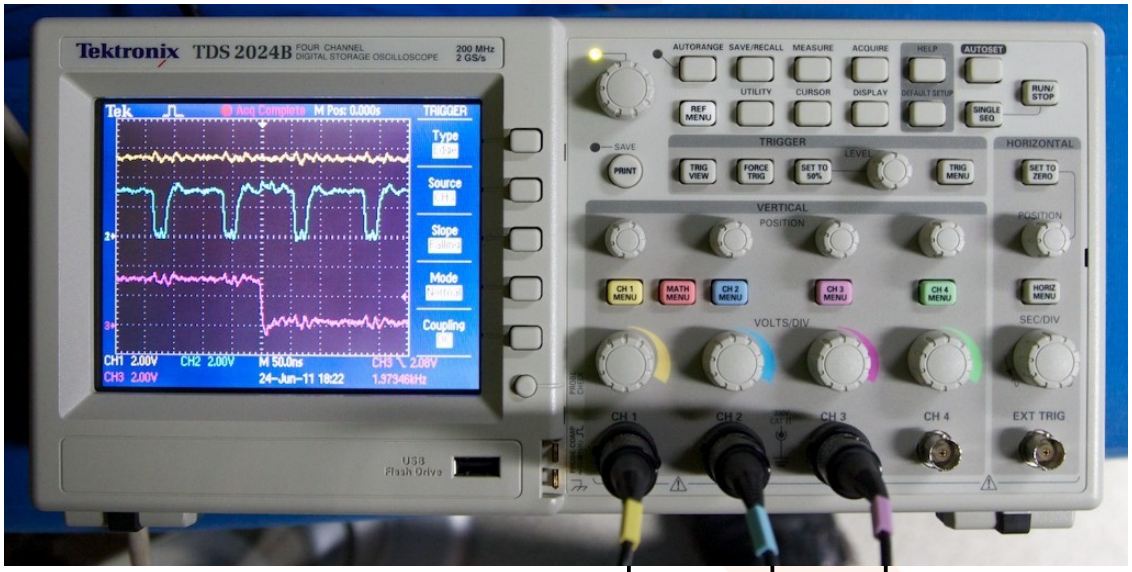
- June 4th, 2011:
  - ATMEGA128 @ 16 MHz
    - BlinkenWall output code converted from C to assembly
      - Time for picture output improved from ~ 3.5 ms to ~ 0.5 ms
    - SRAM (4 kB) < 8 grayscale frame (~ 8.5 kB) **:-(**
  - ARM7 @ 70 MHz
    - Access to I/O port takes 8 cycles (~ 114 ns) > 36 ns **:-(**
- June 5th, 2011:
  - Decide to learn VHDL
  - Order an FPGA development board

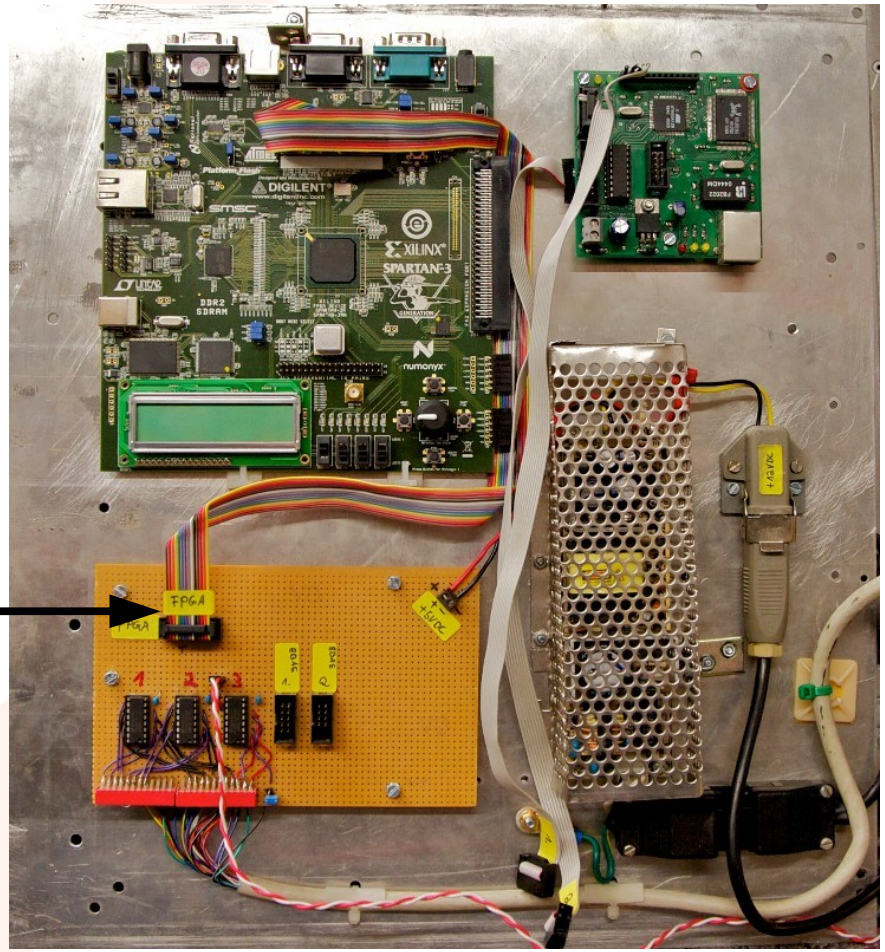
FPGA

- Xilinx Spartan 3
  - 45 kB SRAM
  - 50 MHz
    - Not a very high frequency
    - FPGAs are inherently parallel
      - All computation units can do work in each cycle
      - Every I/O pin can be changed each cycle

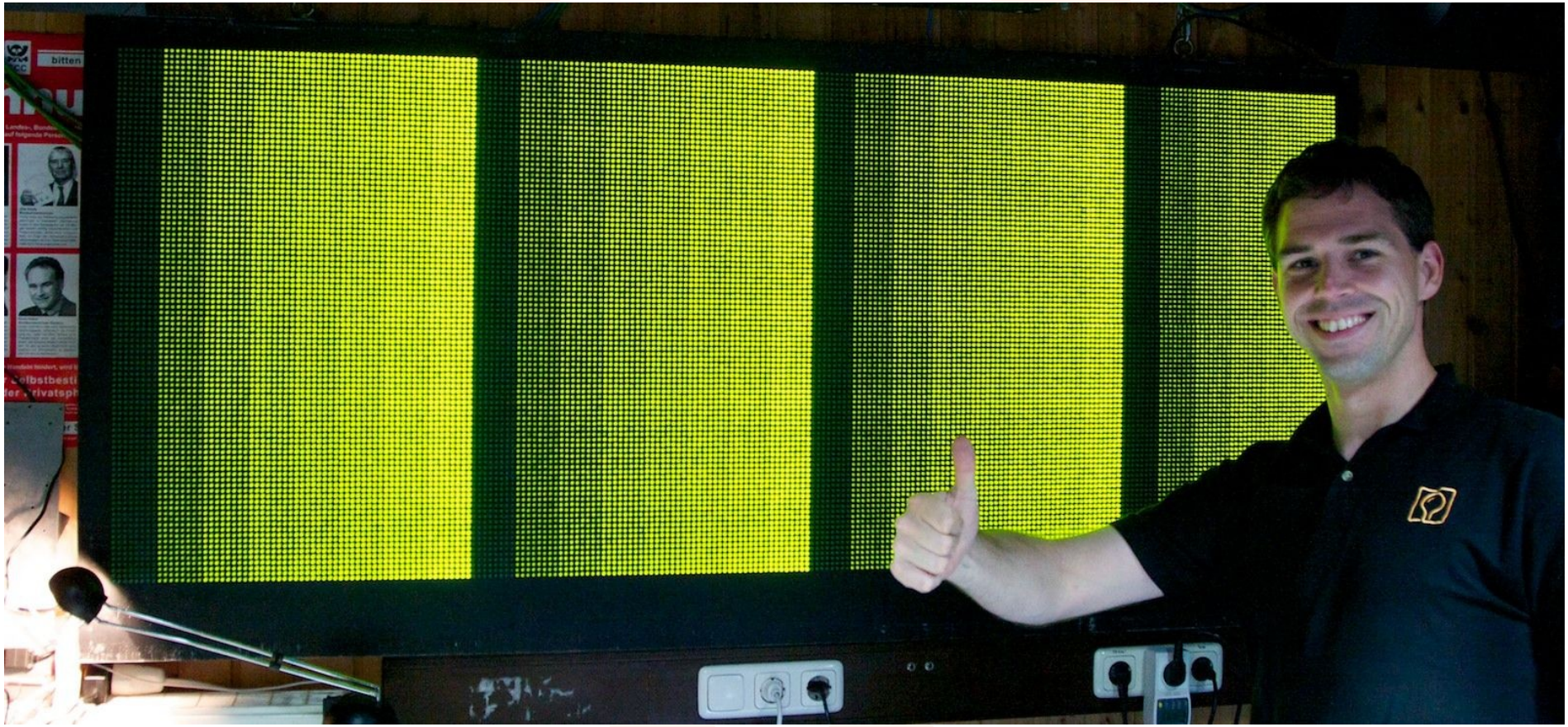


BlinkenWall reloaded Controller



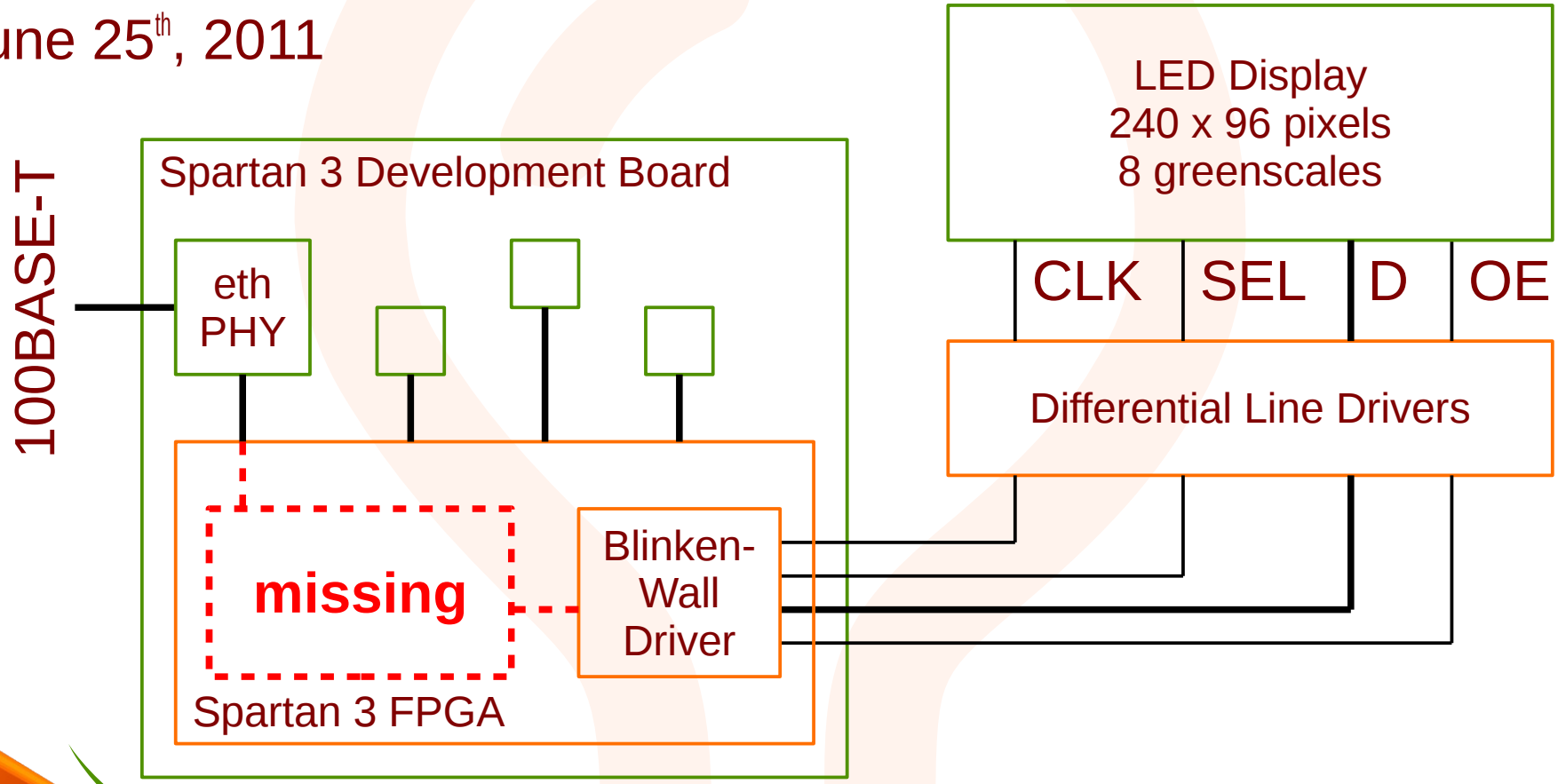


First Greenscales



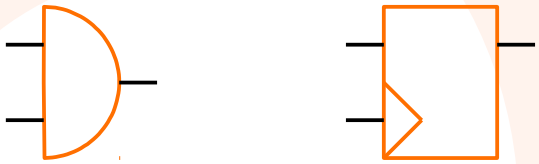
BlinkenWall not yet reloaded

- June 25th, 2011



FPGAs are stupid

- FPGAs can do:
  - logic gates
  - flipflops

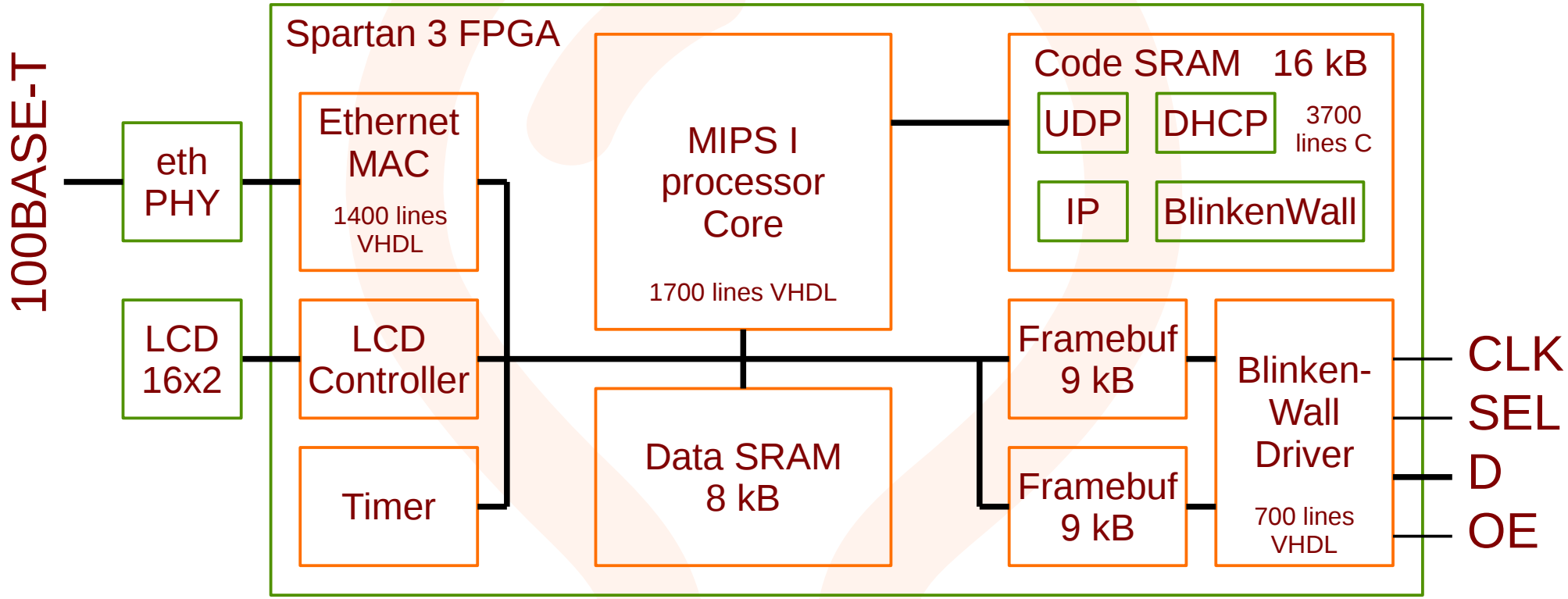


- Implement UDP over IP over Ethernet with just those?
  - I tried... and failed.
- Chaos Communication Camp 2011:
  - BlinkenWall with static greenscale test image
  - Decision: Write a processor in VHDL and run it on the FPGA.

MIPS I processor in VHDL

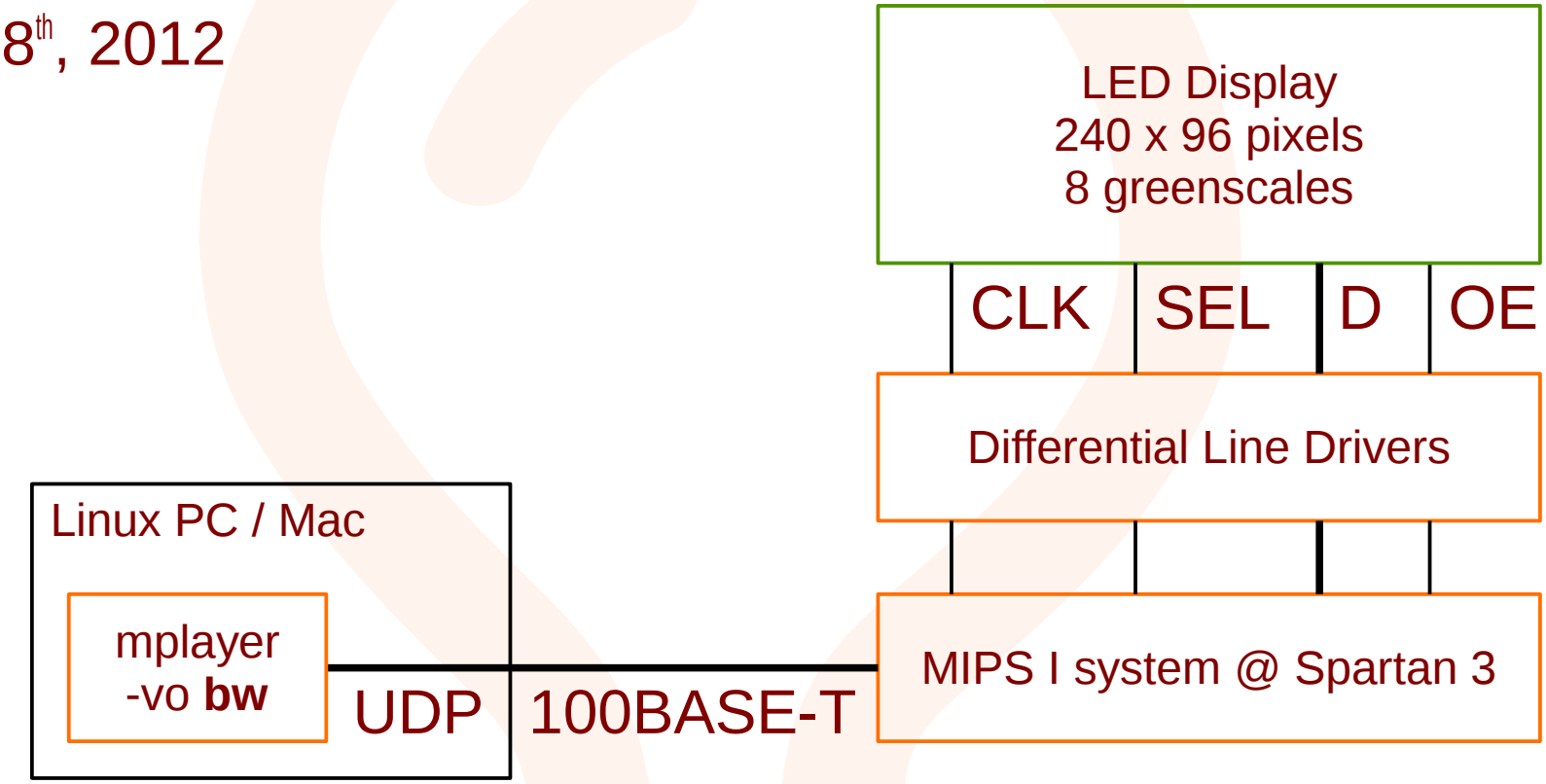
- Why MIPS I?
  - Very simple Instruction Set Architecture
    - RISC: only few, easy instructions
    - no crazy status flags
  - GCC support
    - writing C code is less work than writing assembly code
  - 32 bit
    - higher performance than 8 bit

MIPS I system

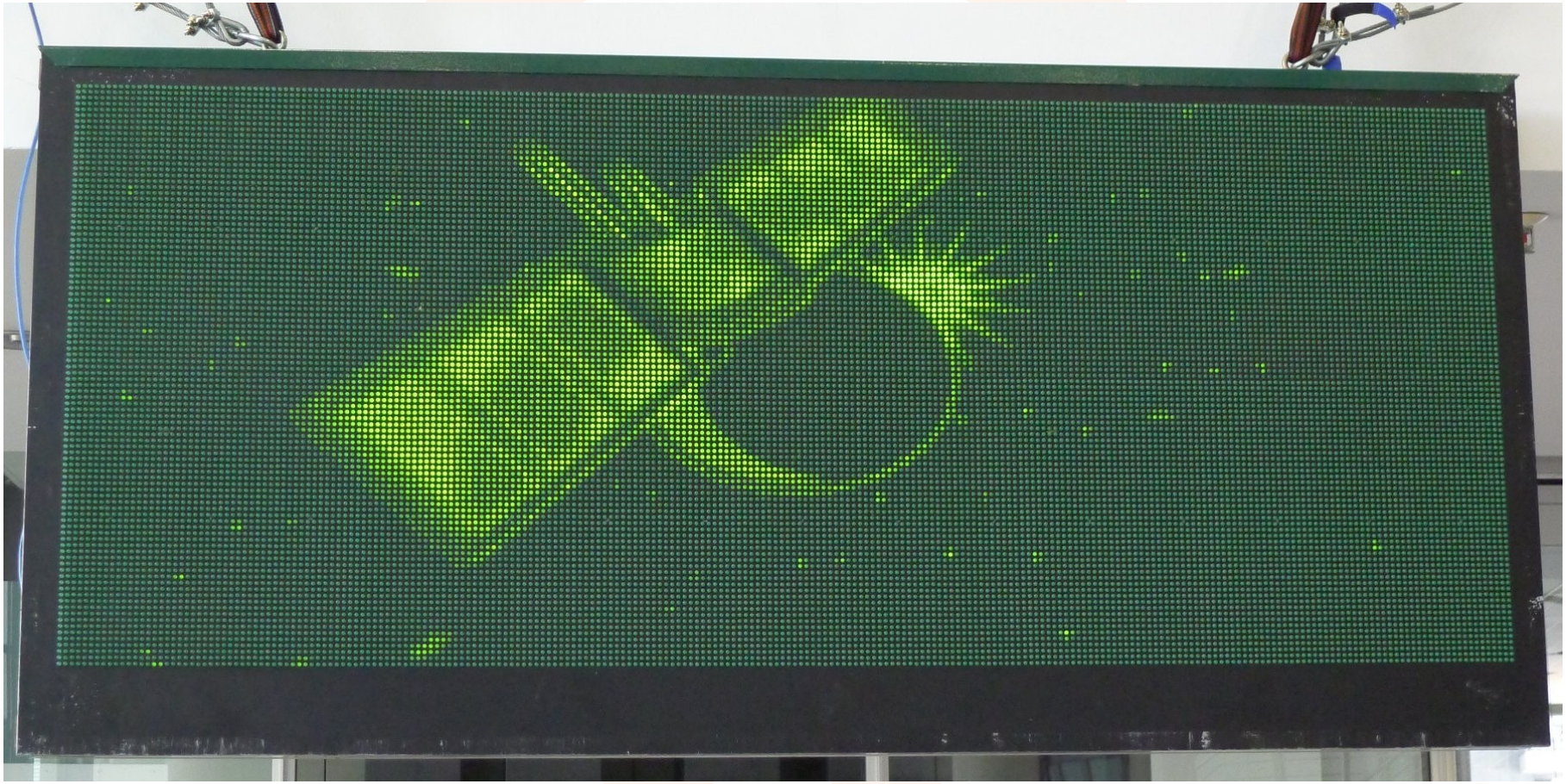


BlinkenWall reloaded

- April 28th, 2012



8 Greenscales Video



Nvision 08 invitation by farbrausch

Thank You!

@LUMINO:	for manufacturing the LED display in 1986
@efelon:	for finding BlinkenWall at Ebay for the presentation template
@ST:	for winning the BlinkenWall auction at Ebay
@POC Sascha:	for giving BlinkenWall a home for replacing power supplies and fans for transportation services
@SIGINT 2012:	for accepting this talk
@audience:	for listening